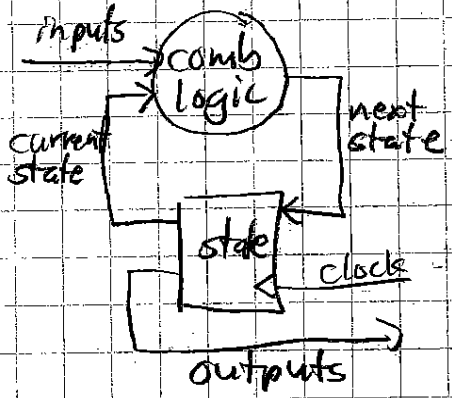
Taxonomy of fixed-connection networks

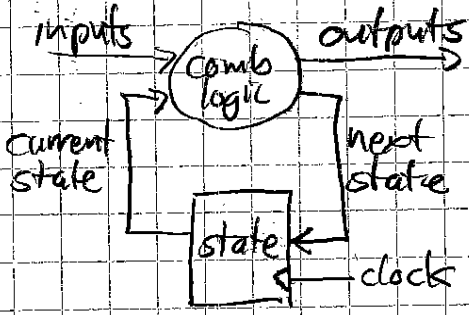
- systolic - all state and interprocessor communication is clocked.
- semisystolic - all state is clocked.
- combinational - no state, no clocks

Finite-state machines

Moore machine



Mealy machine



A systolic network is a network of Moore machines.
A semisystolic " " " " " Mealy "
(with no comb loops).

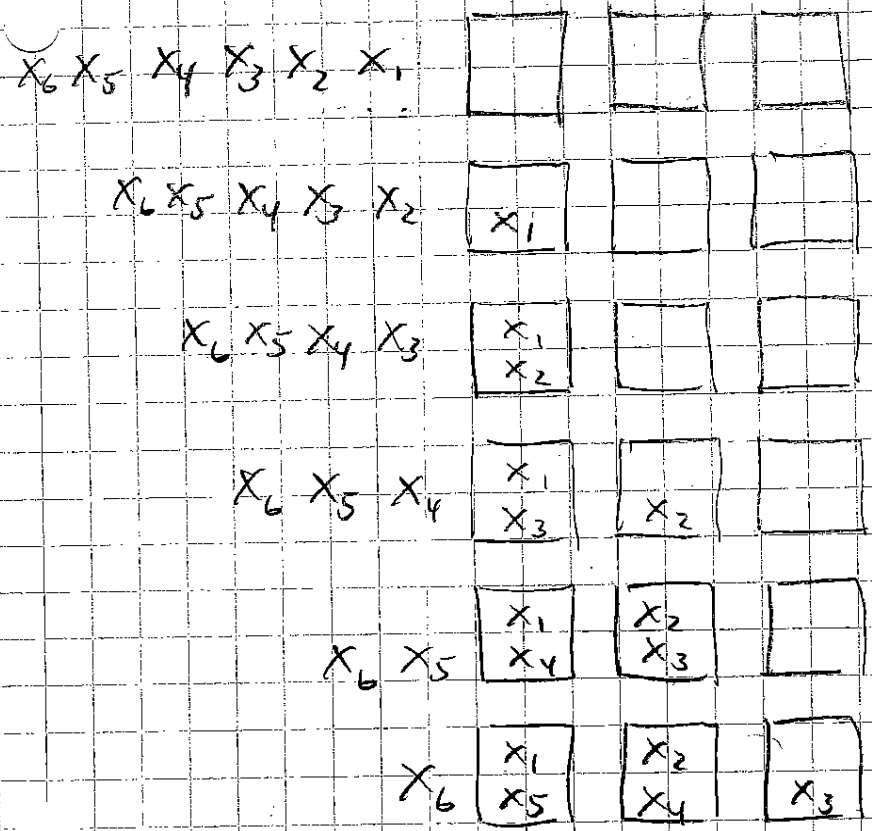
Example. Semisystolic palindrome recognizer
(Palindrome if $x = x^R$ ← reverse)
Takes seq. $\langle x_1, x_2, \ldots \rangle$ as input. Produces $\langle y_1, y_2, \ldots \rangle$ as output, where

$$y_i = \begin{cases} 1 & \text{if } x_1 x_2 \ldots x_i \text{ is a palindrome} \\ 0 & \text{otherwise.} \end{cases}$$

E.g. $x = \langle a, b, a, c, a, b, a \rangle$
$y = \langle 1, 0, 1, 0, 0, 0, 1 \rangle$

Semisystolic network

- systolic + global comb logic

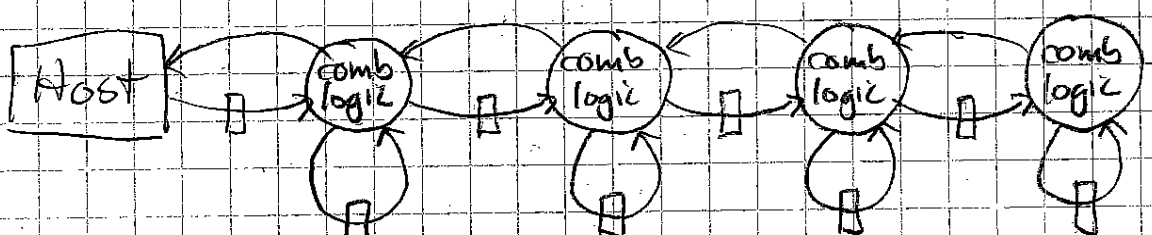


Each cell compares its two values.
Ripple a global AND from right to left.

Real time: On same tick that x_i is input, y_i is output.

Only trouble: long clock period.
$\Theta(N)$ for N-cell array.

Abstract view of circuit

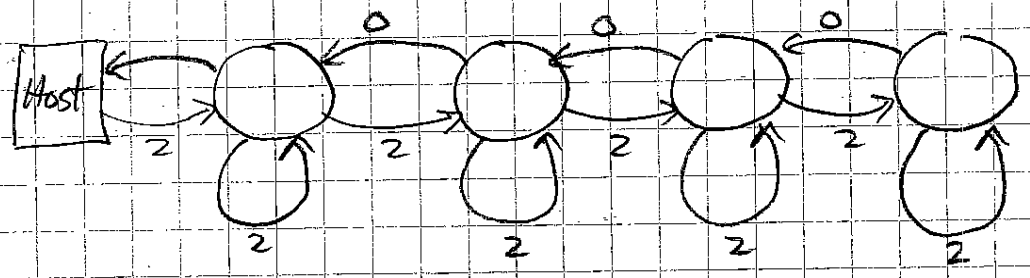


6.896
2/23/04
L6.3

Semisystolic: ≥ 0 registers on each edge
Systolic ≥ 1 register on each edge → + no 0-weight cycles

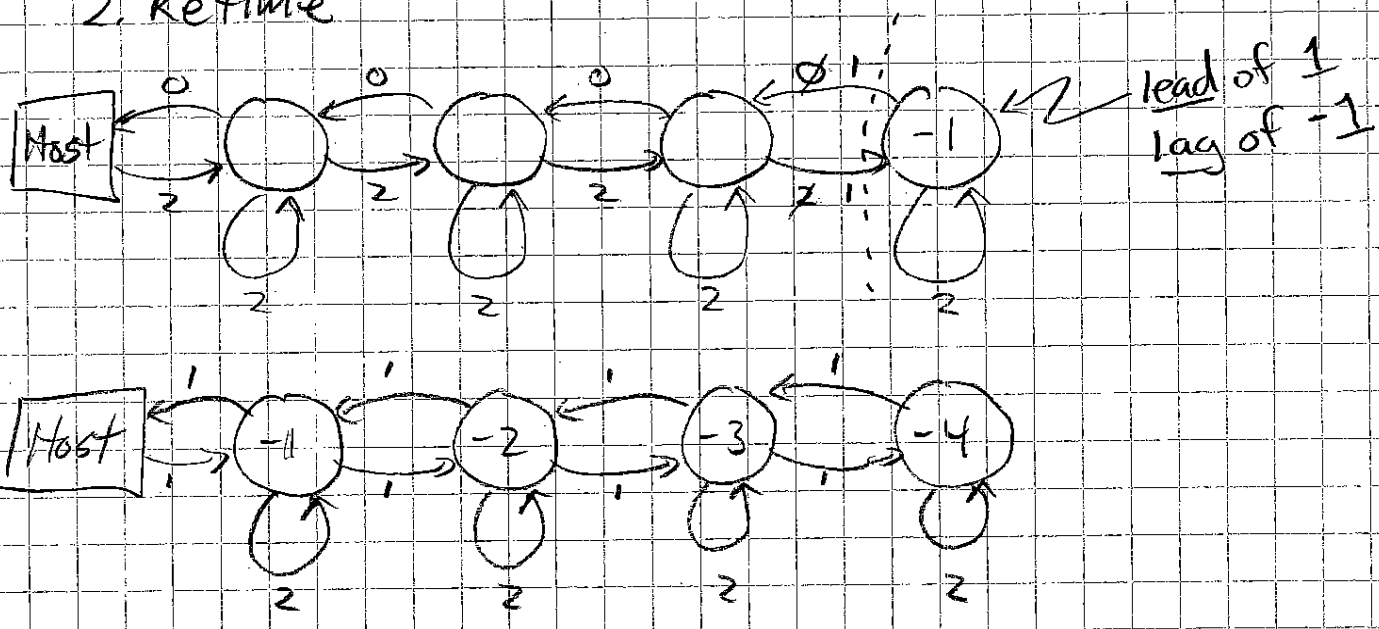
Transformation techniques

1. Slowdown: Double register counts



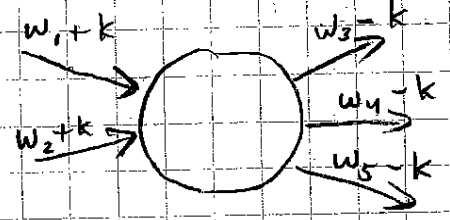
Same function as original semisystolic circuit, but clock twice.

2. Retime

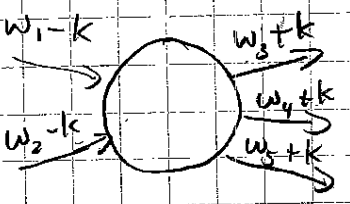


Systolic! Same functionality as doubled semisystolic circuit, but no long comb. delays.
- Initialization may differ.

Retiming a node

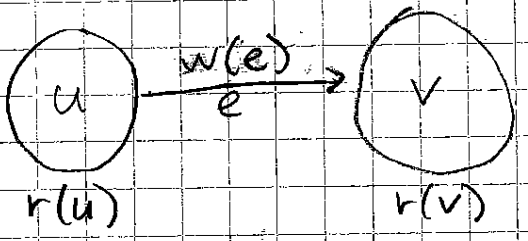


lag of $r(v) = k$



lag of $r(v) = -k$

Retimed edge weights must be ≥ 0.



$$w_r(e) = w(e) - r(u) + r(v)$$

Def. Let $G = (V, E, w)$ be edge-weighted digraph, where $w(e) \geq 0 \ \forall e \in E$. A retiming of G is a mapping $r: V \to \mathbb{Z}$. The retimed graph is $G_r = (V, E, w_r)$, where $w_r(e) = w(e) - r(u) + r(v) \ \forall e \in E$. The retiming is legal if $w_r(e) \geq 0 \ \forall e \in E$.

Note: Normally, we assume $r(\text{Host}) = 0$.

Lemma. Let $G=(V,E,w)$ be circuit, and let $r: V \to \mathbb{Z}$ be retiming. Then, for any path $u \xrightarrow{p} v$ in G, we have

$$w_r(p) = w(p) - r(u) + r(v).$$

Pf. Sup. p is $v_0 \xrightarrow{e_0} v_1 \xrightarrow{e_1} \cdots \xrightarrow{e_{k-1}} v_k$.

$$\begin{aligned} w_r(p) &= \sum_{i=0}^{k-1} w_r(e) \\ &= \sum_{i=0}^{k-1} (w(e_i) - r(v_i) + r(v_{i+1})) \\ &= \sum_{i=0}^{k-1} w(e_i) + \sum_{i=0}^{k-1} (-r(v_i) + r(v_{i+1})) \\ &= w(p) - r(v_0) + r(v_k) \quad \text{(telescope)} \end{aligned}$$ ☒

Corollary. For any cycle p, $w_r(p) = w(p)$. ☒

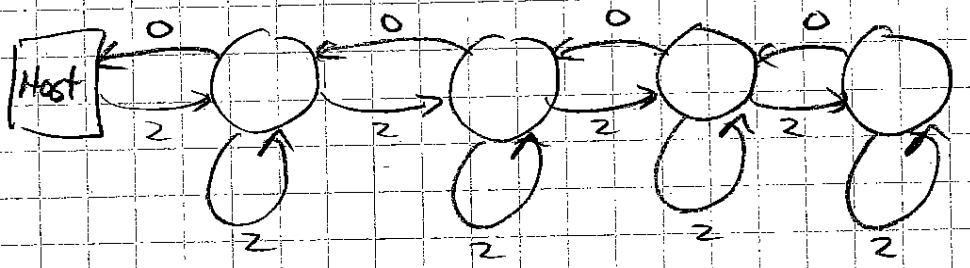
Theorem (Systolic conversion)

Let $G=(V,E,w)$ be a semisystolic circuit, and define $G-1 = (V,E,w')$, where $w'(e) = w(e) - 1$ $\forall e \in E$. Then, $\exists$ legal retiming $r: V \to \mathbb{Z}$ of G such that G_r is systolic iff $G-1$ has no negative-weight cycles.

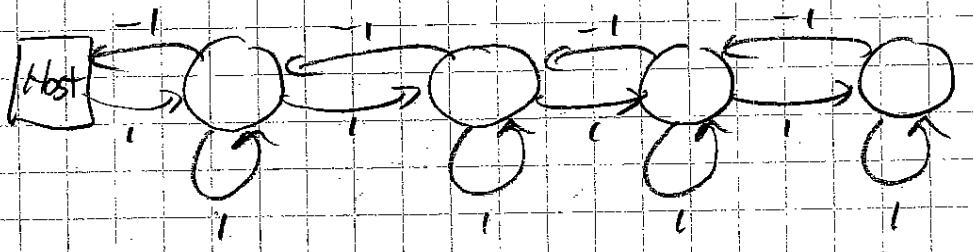
the "constraint graph"

Example

G:



G-1:



No neg-wt. cycles.

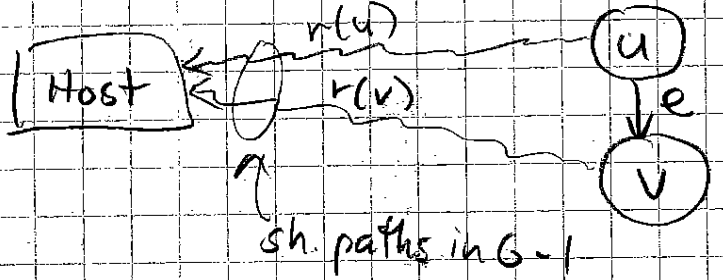
Proof.

($\Leftarrow$) Sup. G-1 has no neg-wt cycles.

Define $r(v)$ = wt of shortest path from v to host in G-1

Note: $r(v)$ defined, since G-1 has no neg-wt. cycles.

Claim: $\forall\ u \xrightarrow{e} v \in E$, $w_r(e) = w(e) - r(u) + r(v) \geq 1$.



Δ-ineq: $r(u) \leq w(e) - 1 + r(v)$

- $r(u)$: sh. path from u in G-1
- $w(e) - 1$: wt. of e in G-1
- $r(v)$: sh. path from v in G-1.

Rewrite: $w_r(e) = w(e) - r(u) + r(v) \geq 1$.

($\Leftarrow$) Sup. $G-1$ has neg.-wt cycle $v_0 \xrightarrow{e_0} v_1 \to \cdots \to v_k \xrightarrow{e_k} v_0$

Then $\sum_{i=0}^{k} (w(e_i) - 1) < 0$

$\Rightarrow \sum_{i=0}^{k} w(e_i) < k.$

But, $\sum_{i=0}^{k} w_r(e_i) \geq k$, and $\sum_{i=0}^{k} w_r(e_i) = \sum_{i=0}^{k} w(e_i)$.

Contradiction. $\boxtimes$