"VLSI"

Now we switch gears and talk about the physical design of circuits. Circuits take area on a chip, or volume in a computer. The goal is to draw analyze circuits, we can analyze circuits for their area just like for their time.

VLSI circuits are drawn with rectangles.

Sidebar: Red Color Code
- polysilicon: RED
- N-diffusion: GREEN
- P-diffusion: PEAFF
- Yellow (Waste)

I use MAGIC colors:

When you cross green and red you get a transistor.

The above:
- A = all red
- B = green on top of red
- C = green below red

This is an N-FET because it uses N-diffusion.

3 Regions:
- A = all red area
- B = green above red
- C = green below red

In schematic this is:

```
A [7]
|    |
| A--|
|    |
|    |
|    |
|    |
| L  |
```
N-FET behavior, (A switch)

A=0

Switch open

A=1

Switch closed

A=0

Strong 1

A=1

poor 1

N-FET is only good at transmitting 0's.

P-FET

Cold to sidebars:

P-diffusion Brown (magic)

Green (waste)

Poly

Brown P-diff

P-FET

Opposite behavior

A=0 open

A=0 ⇒ closed, passes 1's well

A=1 ⇒ open

N-FET

A=0 open

A=1⇒ closed, passes 0's well

No bubble = NFET

"active high"
VLSI is a club sandwich

Bottom layer: substrate
next: diffusion + poly
next: metall (blue)
next: metall (purple)

Old Days:
1 or 2 layers of metal
flat wide wires

Now:
20 layers of metal
tall thin wires

Implications: in old days capacitance coupling mostly between wire + substrate. $C = O(Area \ of \ rectangle)$

Now: most metal coupling is between adjacent wires. $C = O(Perimeter \ of \ rectangle)$
Lots of cross talk.
A direct lines connected by vias

Build a 3-D maze of conductor out of metal.

Angles: We'll stick to 90° angles
Modern technology inclu 95° + other angles.

Only a constant factor for analysis:

Design Rules:

1. Minimum line width (to avoid open circuit)
2. Maximum separation

Can be combined to "center-to-center spacing"
Can draw the lines on a grid, + capture all info.
A cross inverter.

Schematic:

\[ A \rightarrow \text{open} \rightarrow \text{Not} \rightarrow \bar{A} \rightarrow \bar{B} \]

How it works

\[ A = 0 \rightarrow \text{open} \rightarrow \bar{B} = 1 \]

The P-FETs are used to pass 1's, the NFETs to pass 0's.
Q: Why would you want a repeater?

A: Transmit long distances, a repeater aligns a pair 1 + restores it to a signal 1.
NAND GATE:

Truth Table

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>X</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Logic Symbol

Electrical Schematic

If A or B is 0 then output is 1, else if A + B are both 1 then output is 0.

Exercise: Design and draw a 2-input NOT gate.
Side Trip: De Morgan's Law

Let $A$ be a circuit comprising inputs, or, and, outputs.
Let $\overline{A}$ be the circuit with all ANDS replaced by ORS, and all
ORS replaced by ANDS.

Then if we add inverts to the inputs and outputs of $\overline{A}$
we get a functionally equivalent to $A$ \[ \text{[De Morgan's Law]} \]

Proof: By induction on circuit size.

Base case:

\[ \text{wire} \equiv \text{wire} \]

\[ \text{AND} \equiv \text{OR} \]

\[ \text{OR} \equiv \text{AND} \]

\[ \text{NOT} \equiv \text{NOT} \]

Inductive step:

\( A = R \rightarrow C \rightarrow C \)

\( \overline{A} \)

By ind. hyp.

\( \overline{R} \rightarrow \overline{C} \rightarrow \overline{C} \)

\( \text{constr. a} \)
A biss trick: \[ F = \overline{A \cdot B + C \cdot D} \]

Need: a path to 0 iff \( F \) is false
a path to 1 iff \( F \) is true

The \( N \)-side (path to 0)

\( N \)-fets create a path where \( \overline{A \cdot B + C \cdot D} \) is false,
i.e. \( A \cdot B + C \cdot D \) is true

\[ \begin{array}{c}
A \\
\hline \\
B \\
\hline \\
C \\
\hline \\
D \\
\end{array} \]

The \( P \)-side: path to 1 if \( \overline{A \cdot B + C \cdot D} \) is true.

Path made of \( P \)-fets, so all inputs must be inverted to turn the p-fets switch on. Use DeMorgan

\[ A \cdot B + C \cdot D \equiv (A + \overline{B}) \cdot (\overline{C} + \overline{D}) \]

Exercise: Design an electrical circuit for
\[ F = \overline{(A + B + C) \cdot D} \]