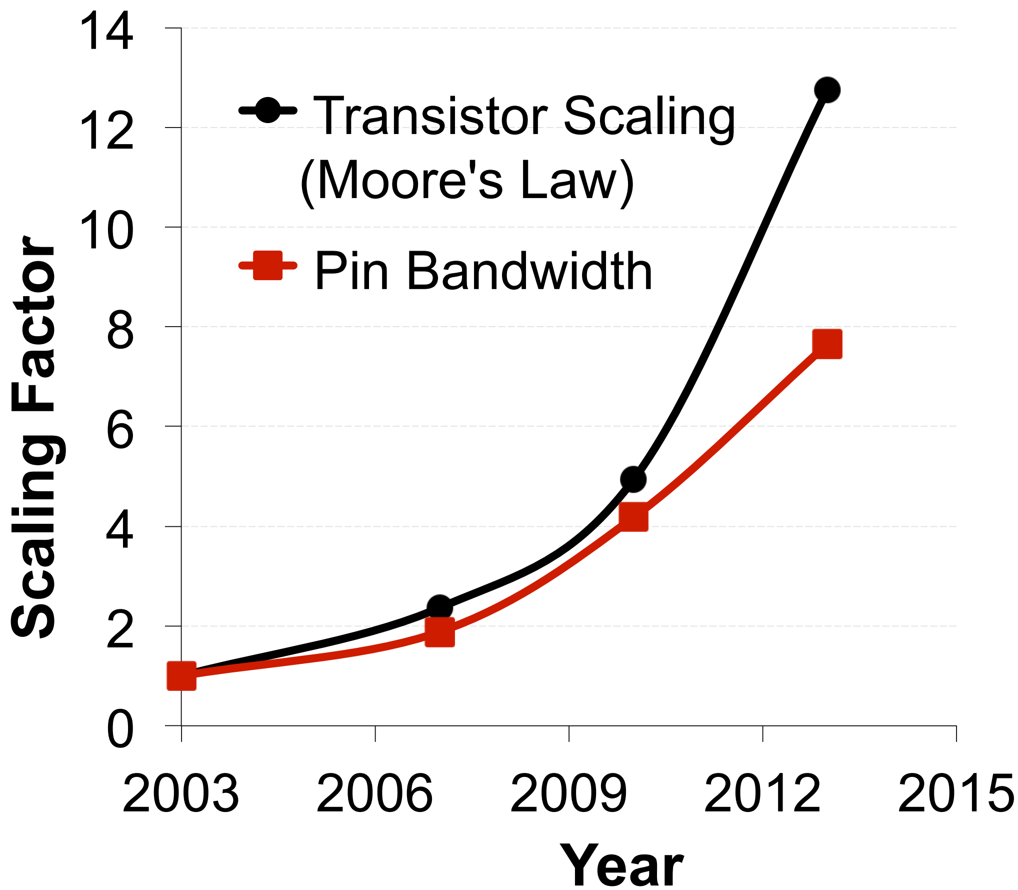
Lecture 20
Future Trends

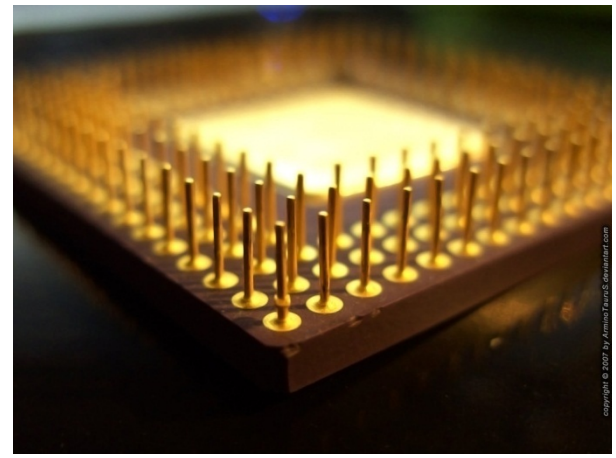
Joel Emer and Daniel Sanchez

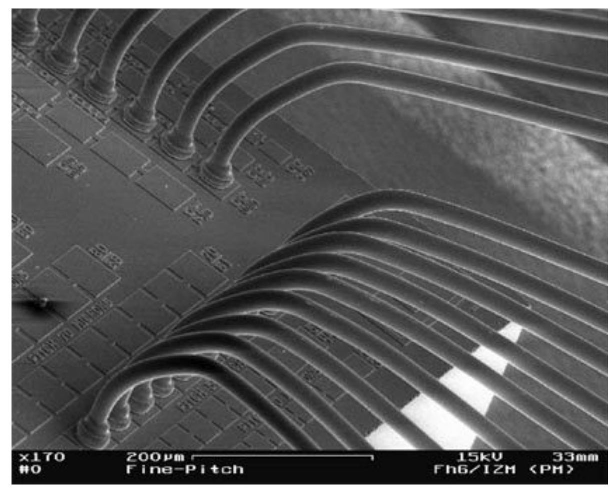
6.888 Parallel and Heterogeneous Computer Architecture
Spring 2013

Massachusetts Institute of Technology

Pin Bandwidth Scaling



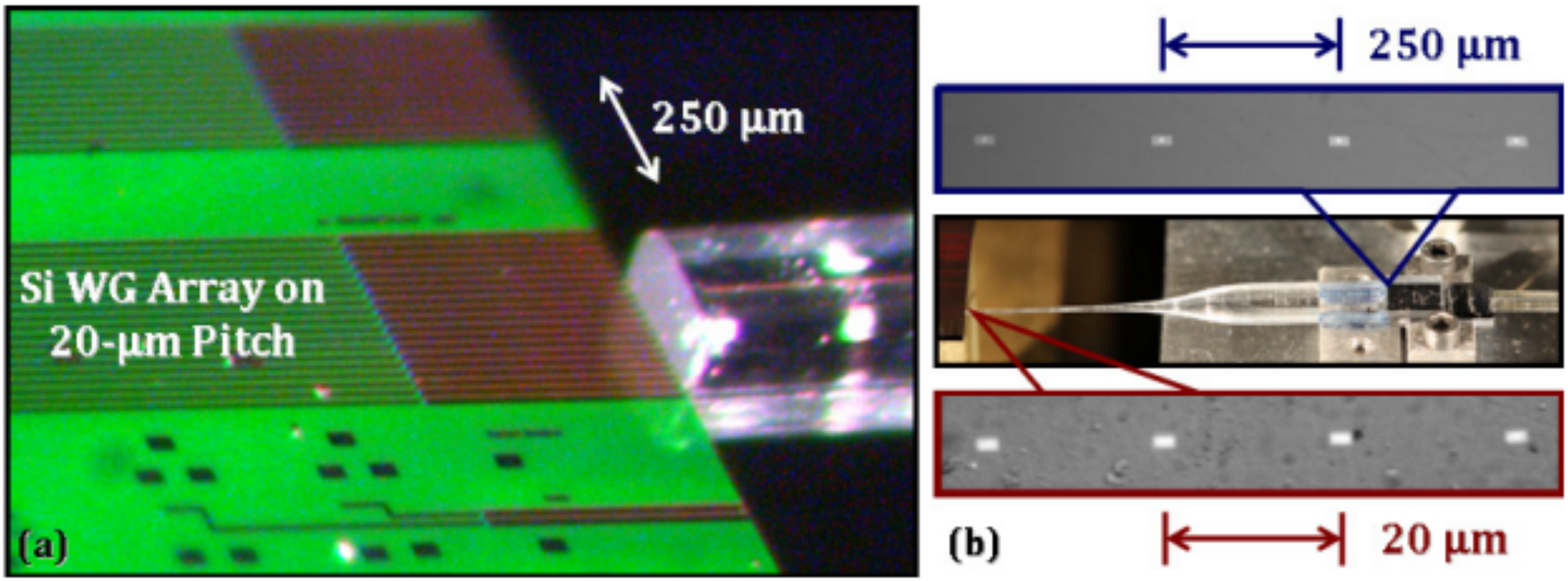




[TU Berlin]

➡ Cannot feed cores with data fast enough to keep them busy

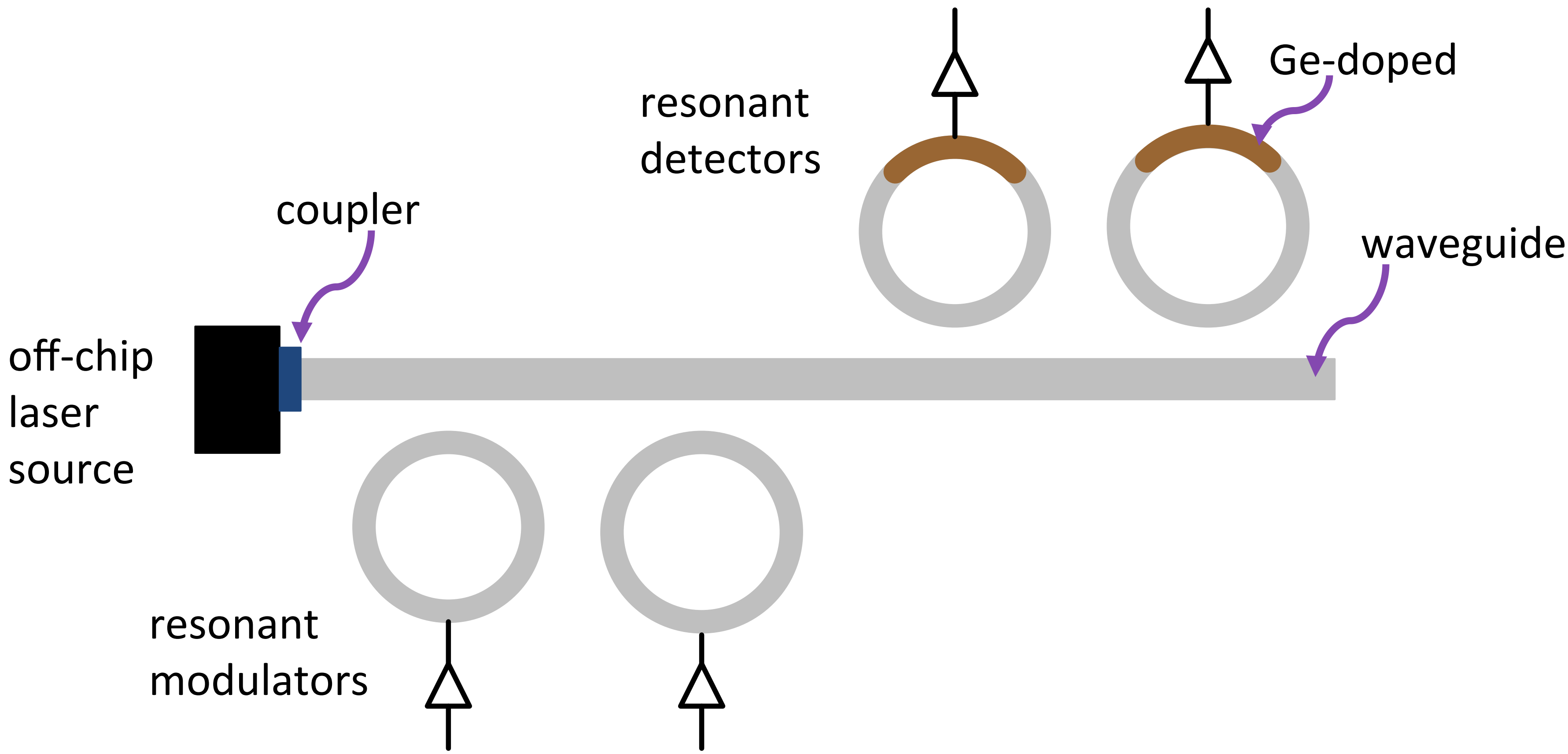
Dense Off-Chip Coupling



- Dense optical fiber array [Lee, OSA/OFC/NFOEC 2010]
- ~3.8*dB* loss, 8 *Tbps/mm* demonstrated
- Misalignment within <0.7 *µm*, 0.4 *µm*, 0.7 *µm*> → loss <1 *dB*

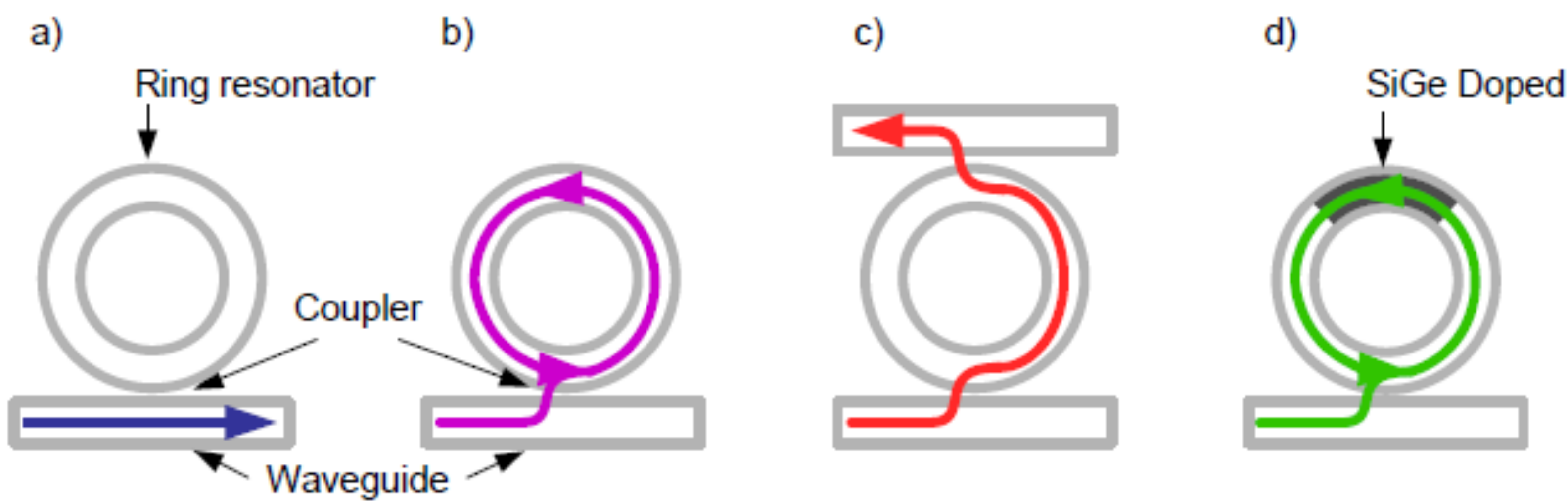
➡ Loss comparable to optical proximity couplers

Nanophotonic Components



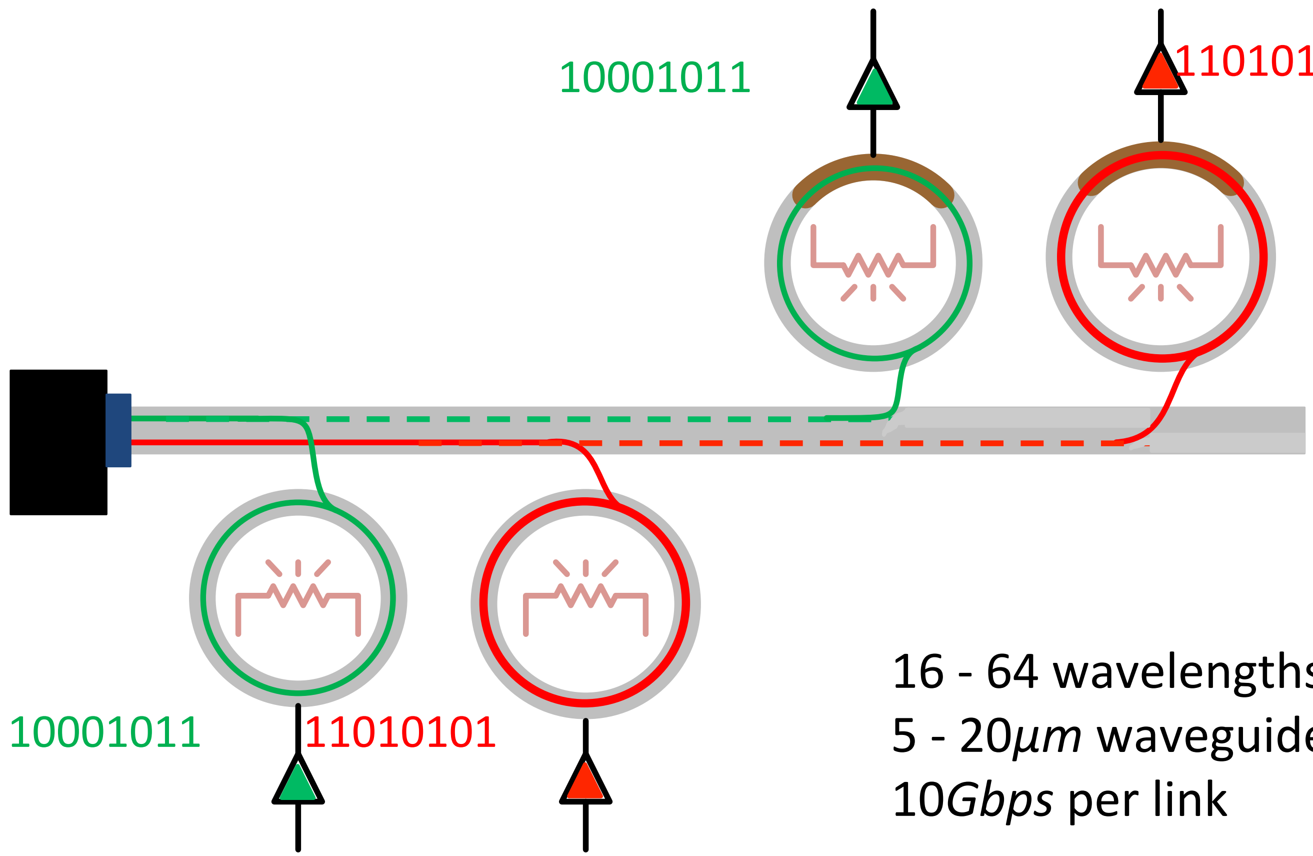
Selective: couple optical energy of a specific wavelength

Modulators/Injectors/Detectors



[Corona]

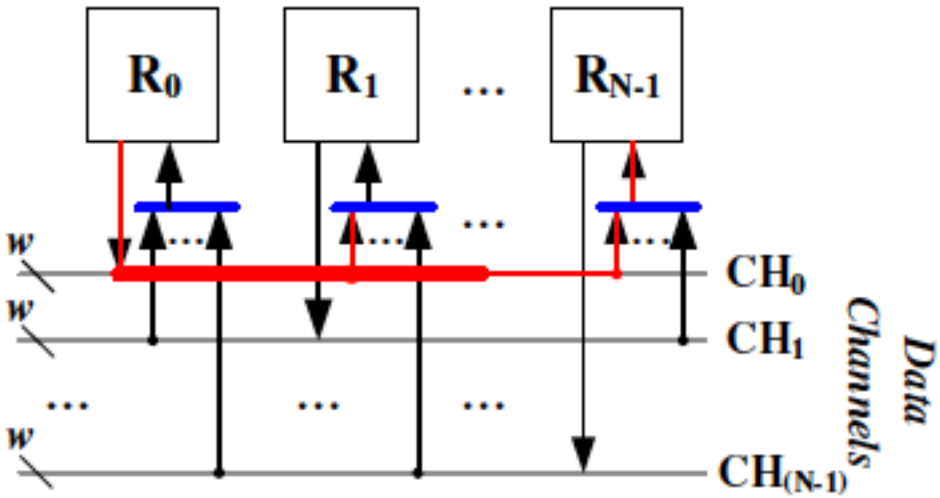
Modulation and Detection



16 - 64 wavelengths DWDM
5 - 20μm waveguide pitch
10*Gbps* per link

➡ 8 Tbps/mm bandwidth density or more !!!

SWMR vs. MWSR Crossbar



Single-Writer Multiple-Reader

Broadcast bus

All receivers always read

On-rings → optical loss

High laser power

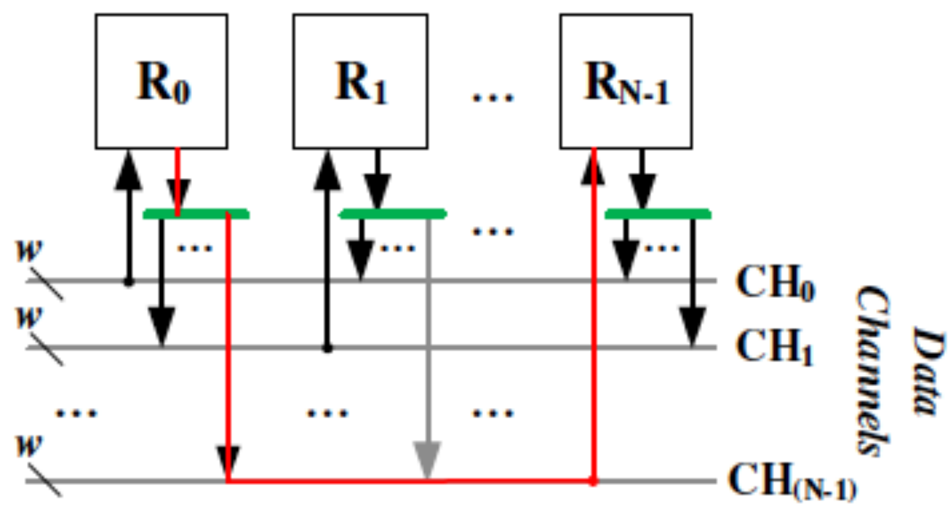
Multiple-Writer Single-Reader

Only one receiver reads

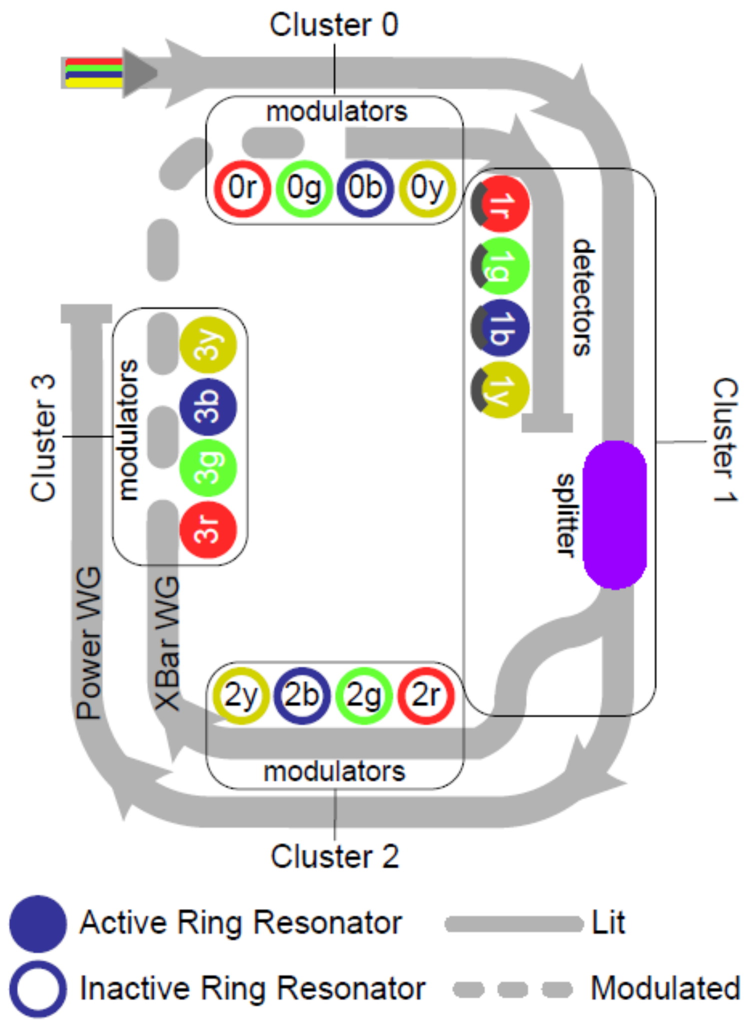
Only one ring is on → low loss

Low laser power

Needs arbitration

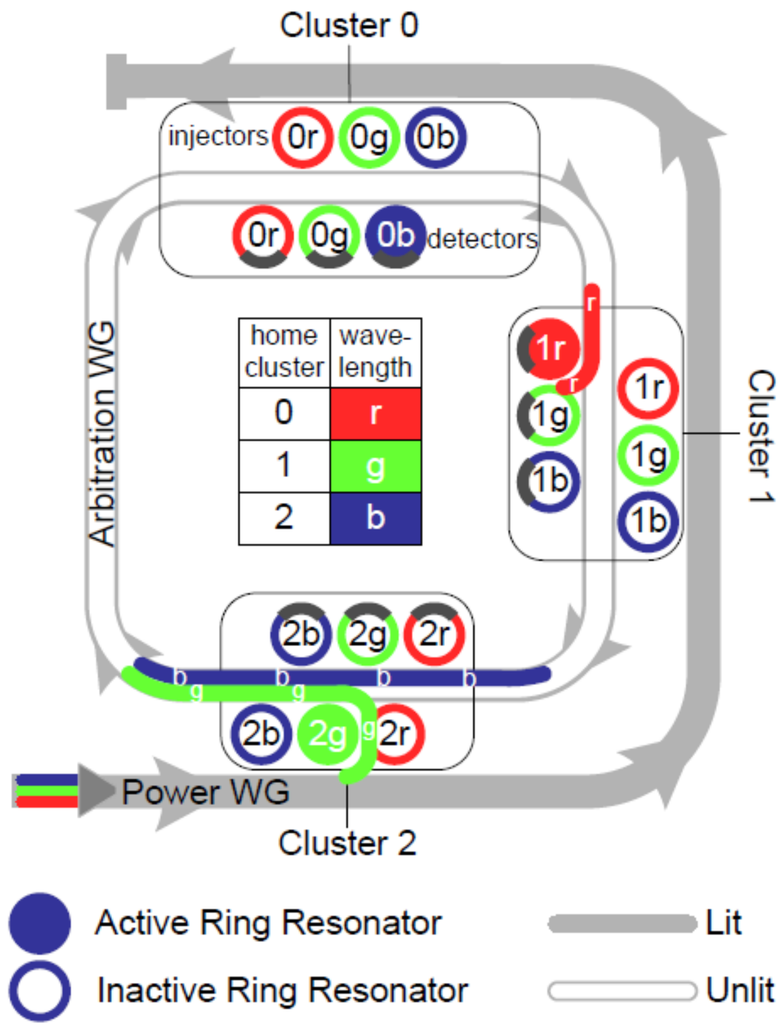


Multi-channel communications



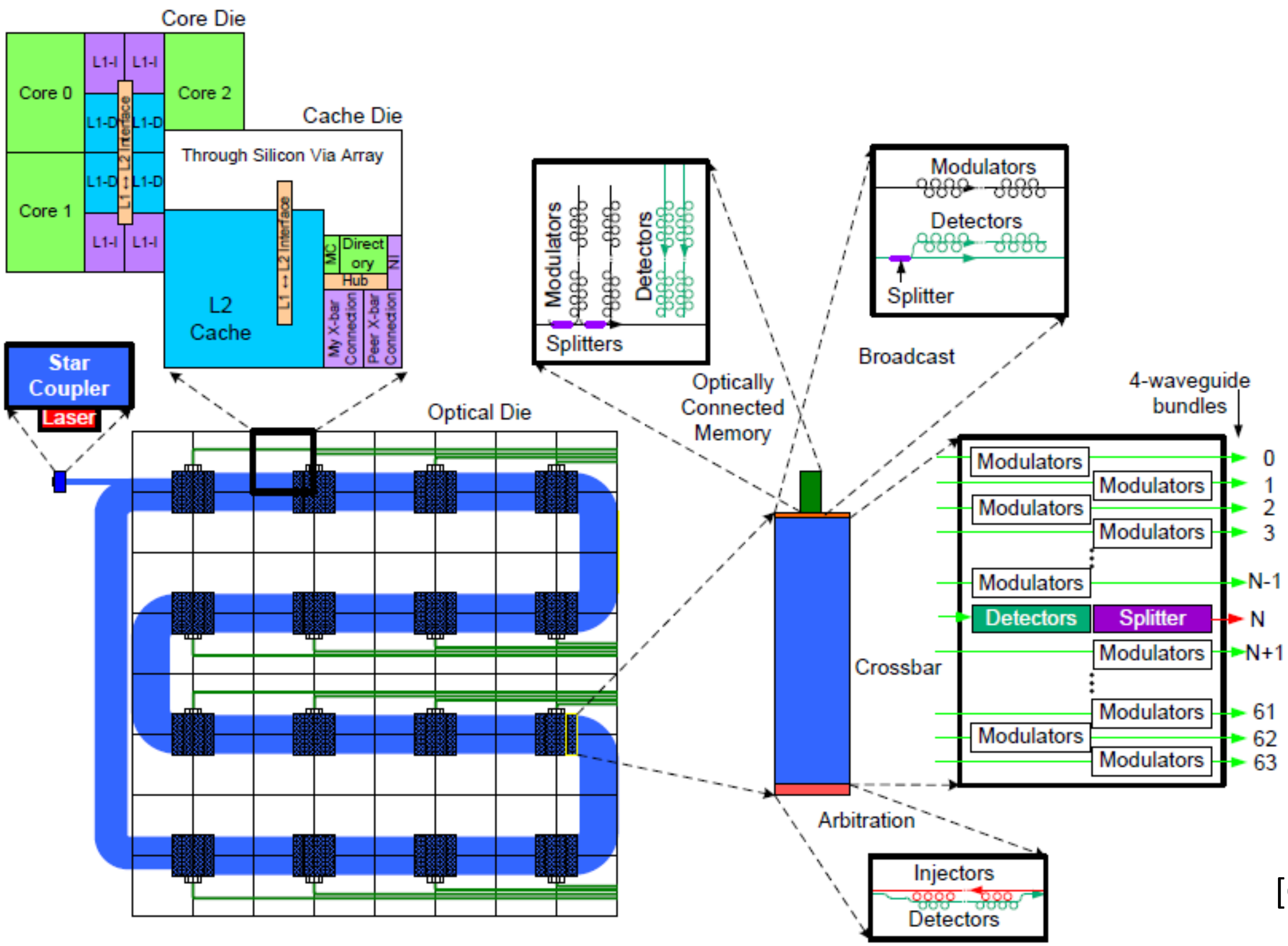
[Corona]

Token-based arbitration



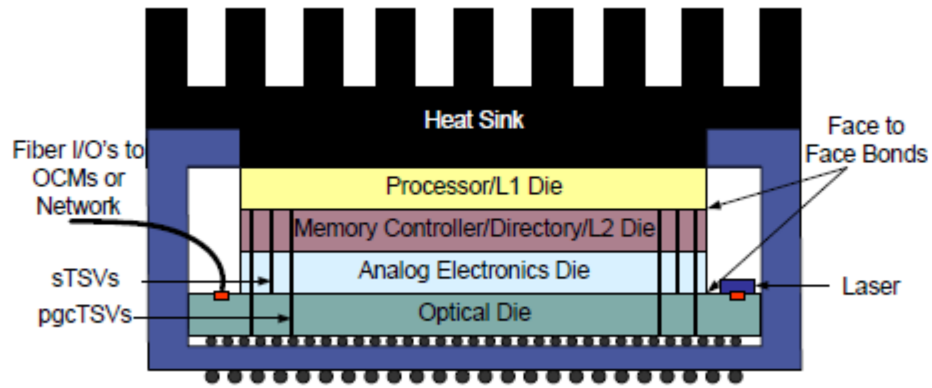
[Corona]

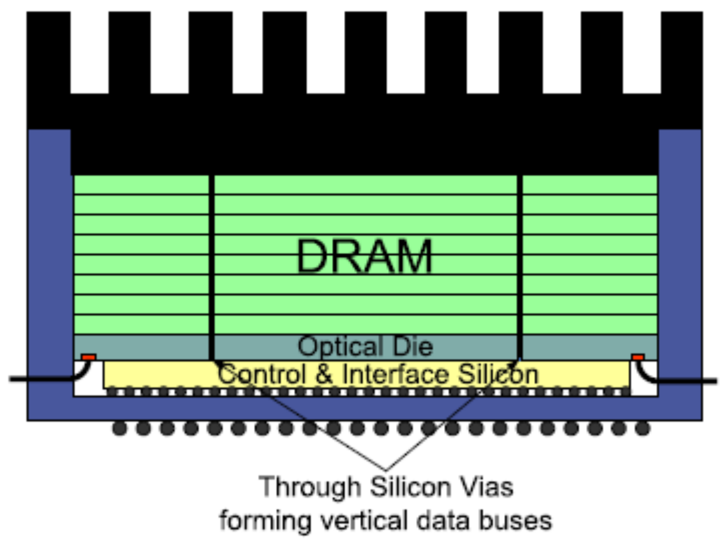
Corona Layout



[Corona]

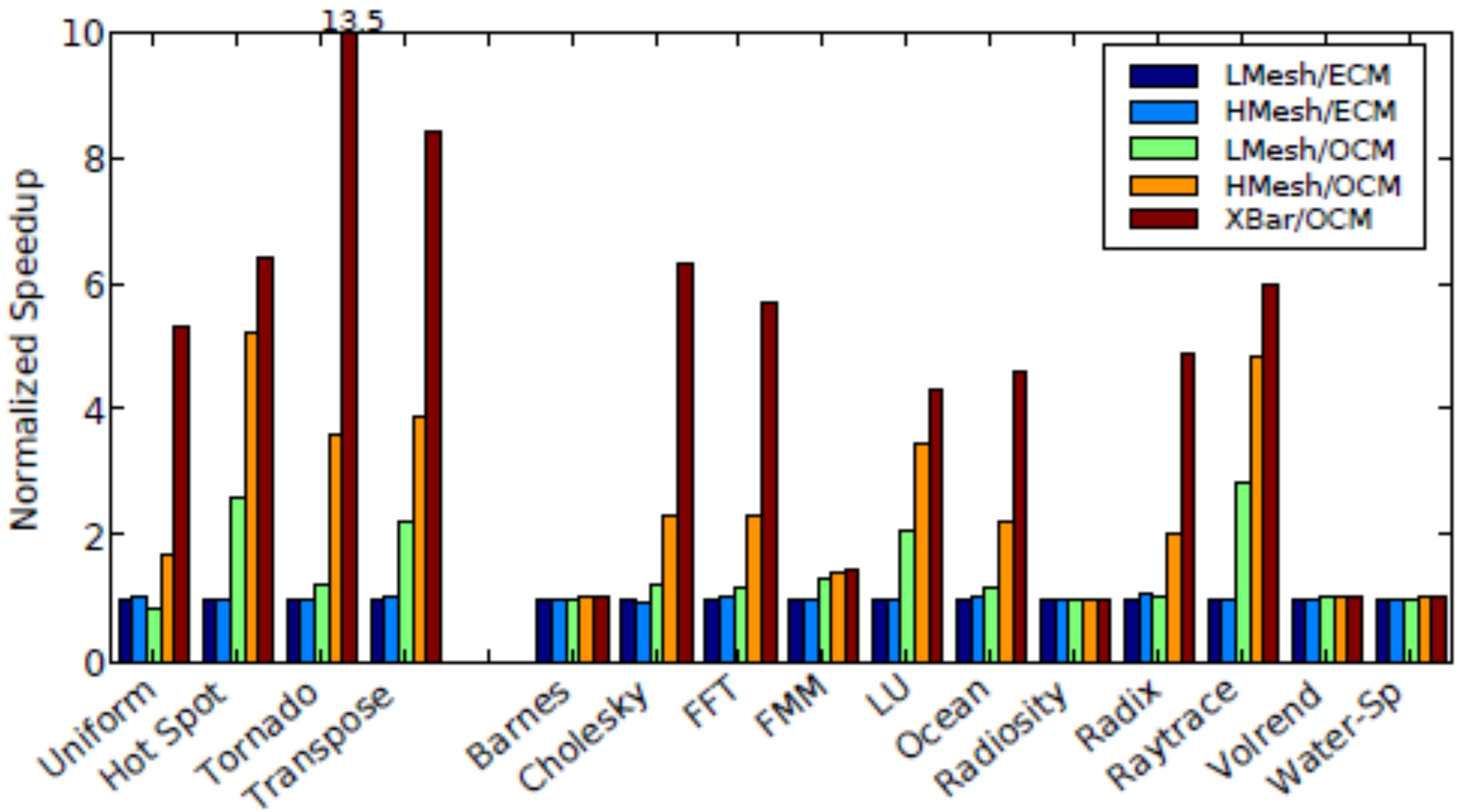
TSV packages





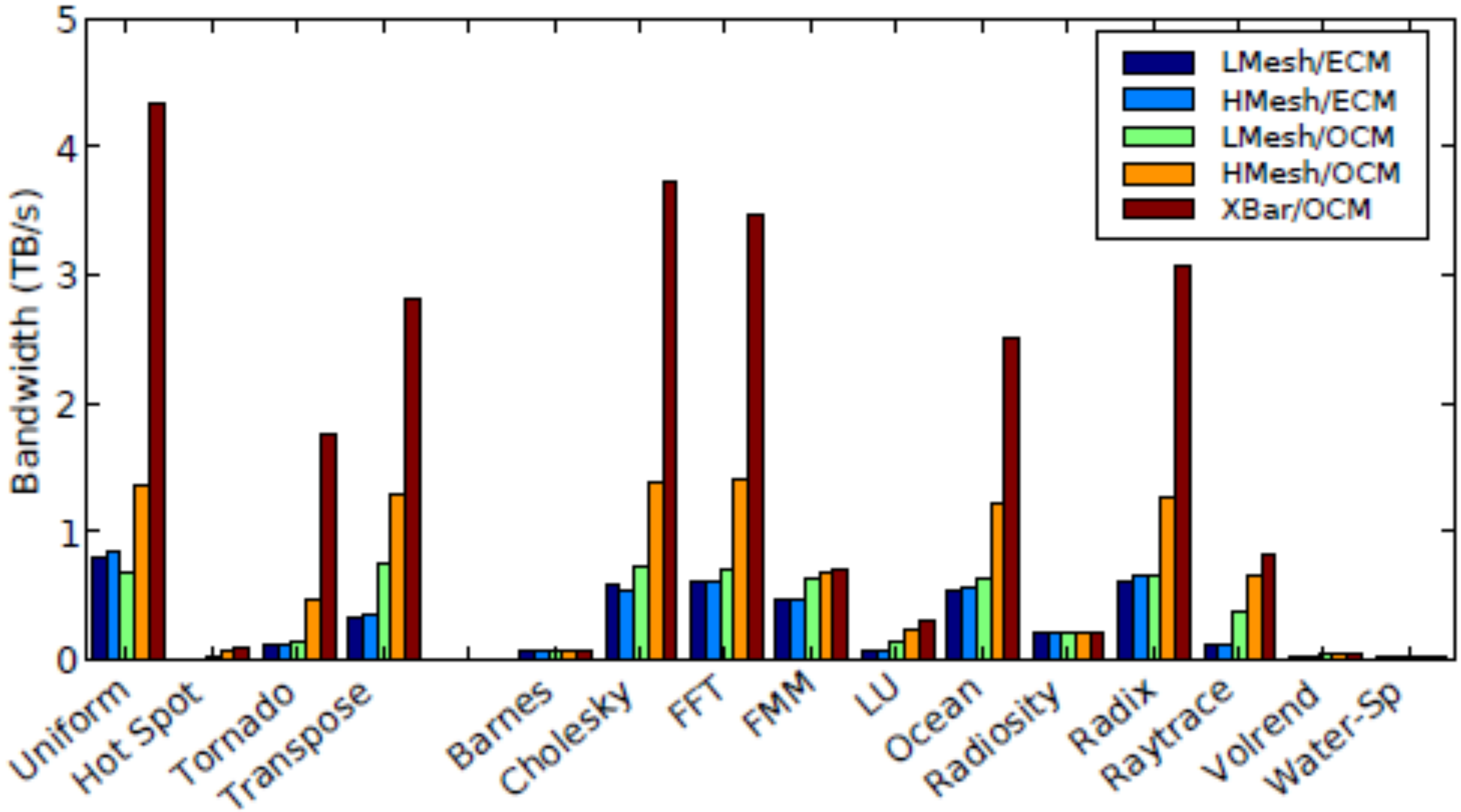
[Corona]

Corona Normalized Speedup

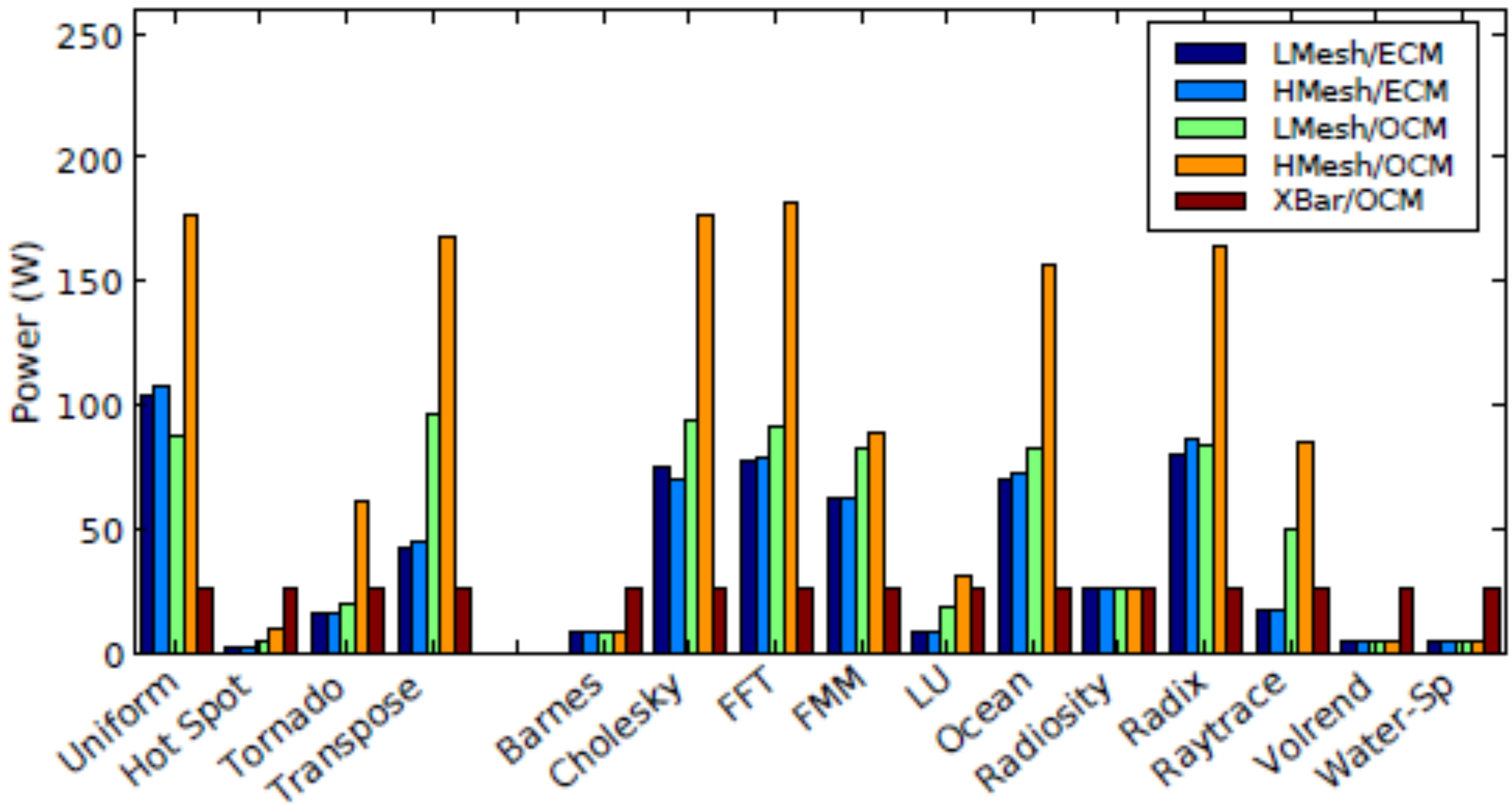


[Corona]

Corona Achieved Bandwidth

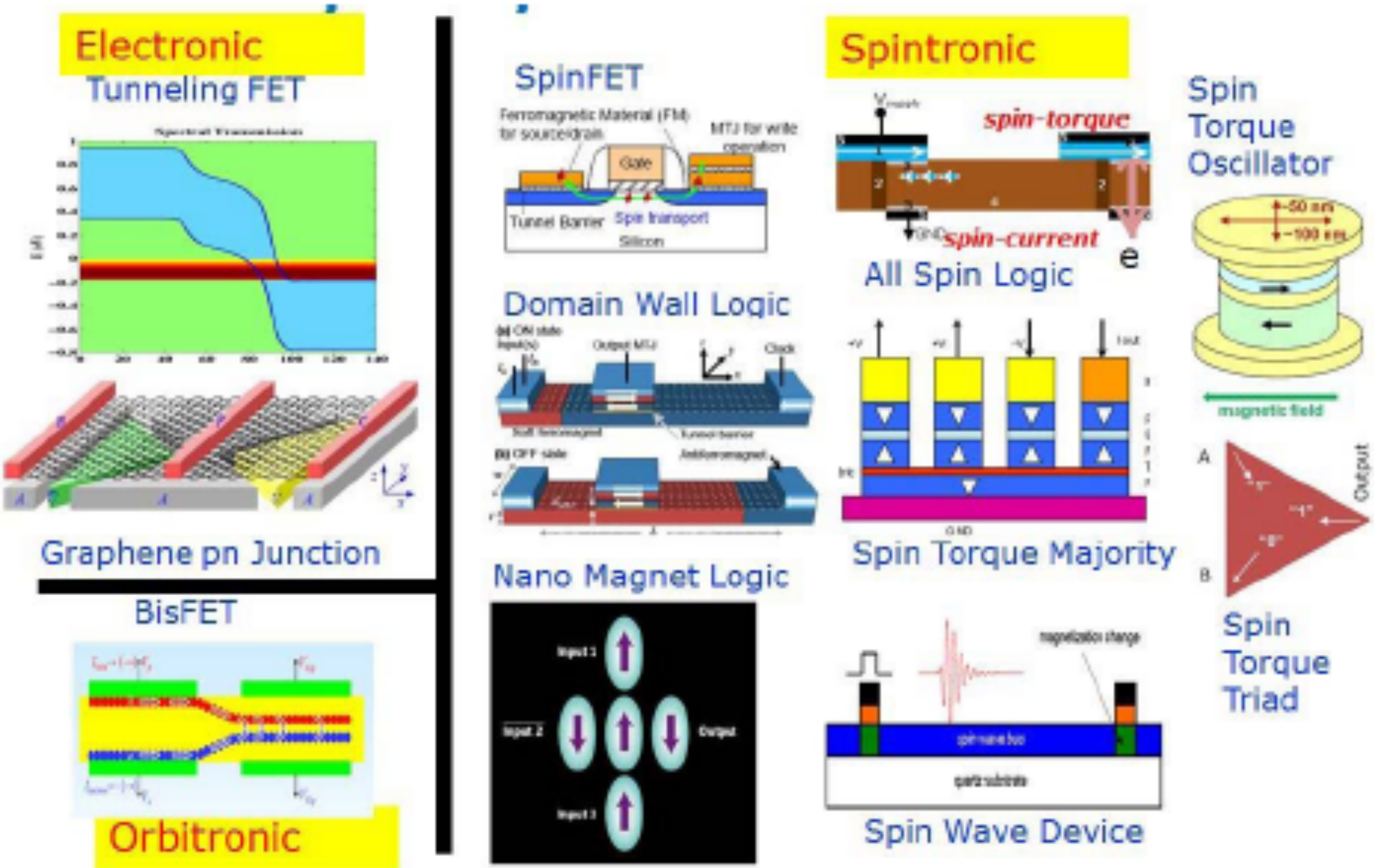


Corona On-chip Network Power



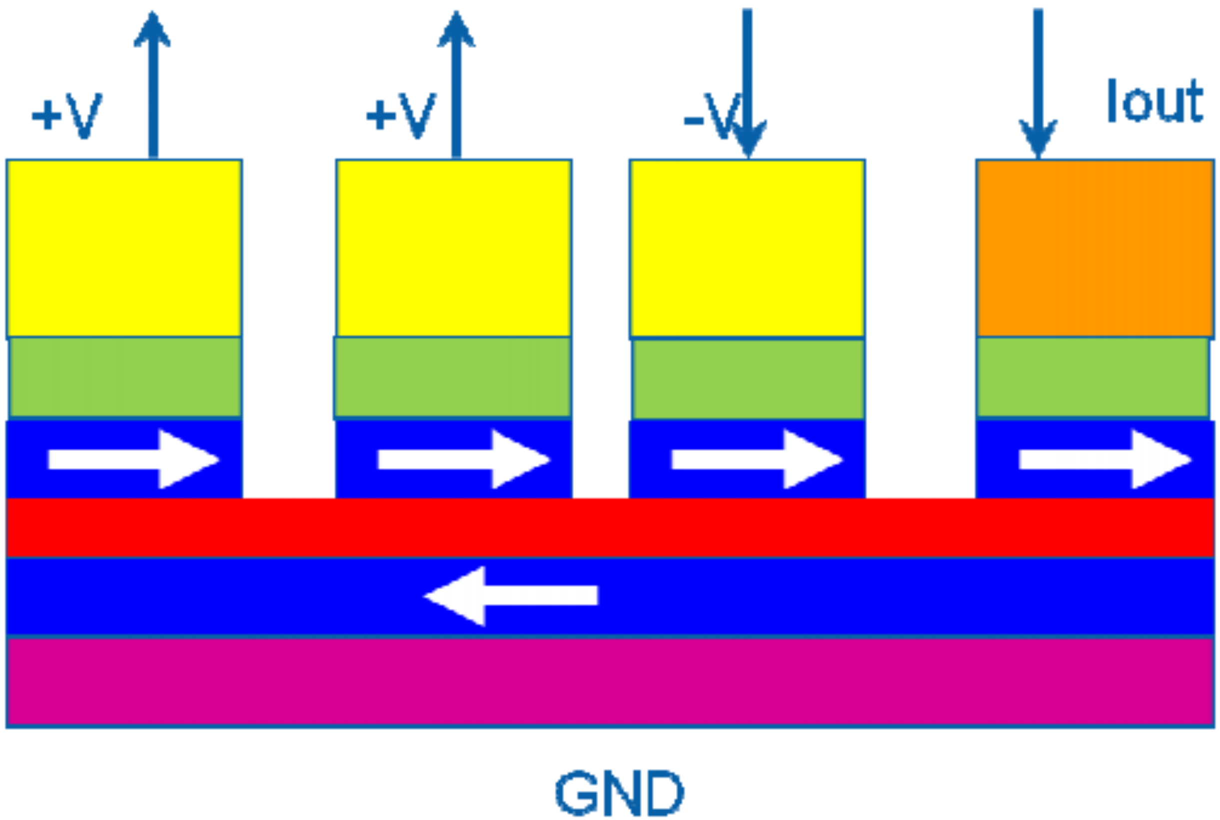
[Corona]

Device Taxonomy



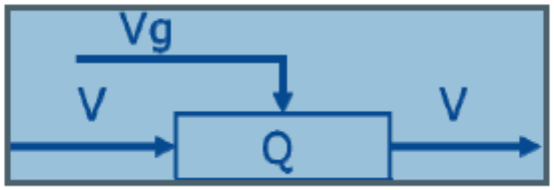
[Beyond CMOS]

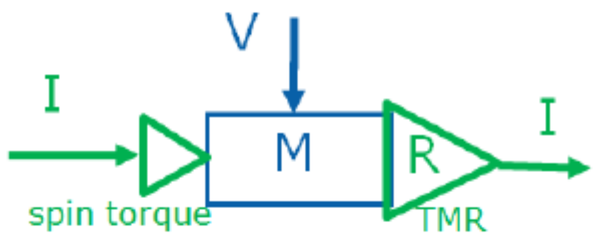
Spin Torque Majority Gate



[Beyond CMOS]

Interfaces Types





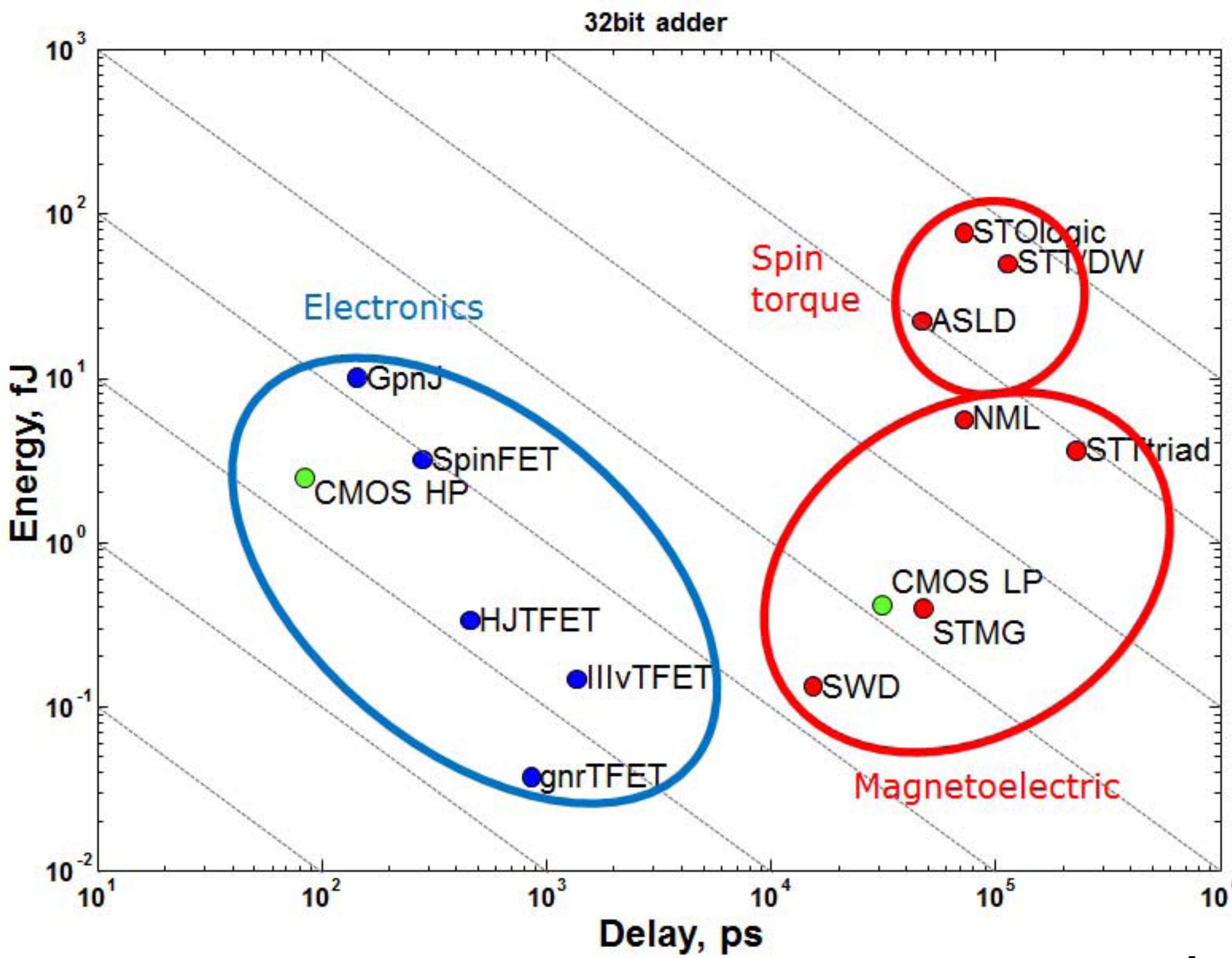
[Beyond CMOS]

Device Characteristics

Device name	acronym	input(s)	control	int. state	output
Si MOSFET high perf.	CMOS HP	V	Vg	Q	V
Si MOSFET low power	CMOS LP	V	Vg	Q	V
III-V tunneling FET	IIIvTFET	V	Vg	R	V
Heterojunction TFET	HJTFET	V	Vg	R	V
Graphene nanoribbon TFET	gnrFTET	V	Vg	R	V
Graphene pn-junction	GpnJ	V	Vg	R	V
Bilayer pseudospin FET	BisFET	V	Vg	BC	V
SpinFET (Sughara-Tanaka)	SpinFET	V	Vg, Vm	Q, M	V
Spin torque domain wall	STT/DW	I	V	M	I
Spin torque majority gate	STMG	M	V	M	M
Spin torque triad	STTtriad	I	V	M	I
Spin torque oscillator	STO	I	V	M	I
all spin logic device	ASLD	M	V	M	M
spin wave device	SWD	M	I or V	M	M
nanomagnetic logic	NML	M	B or V	M	M

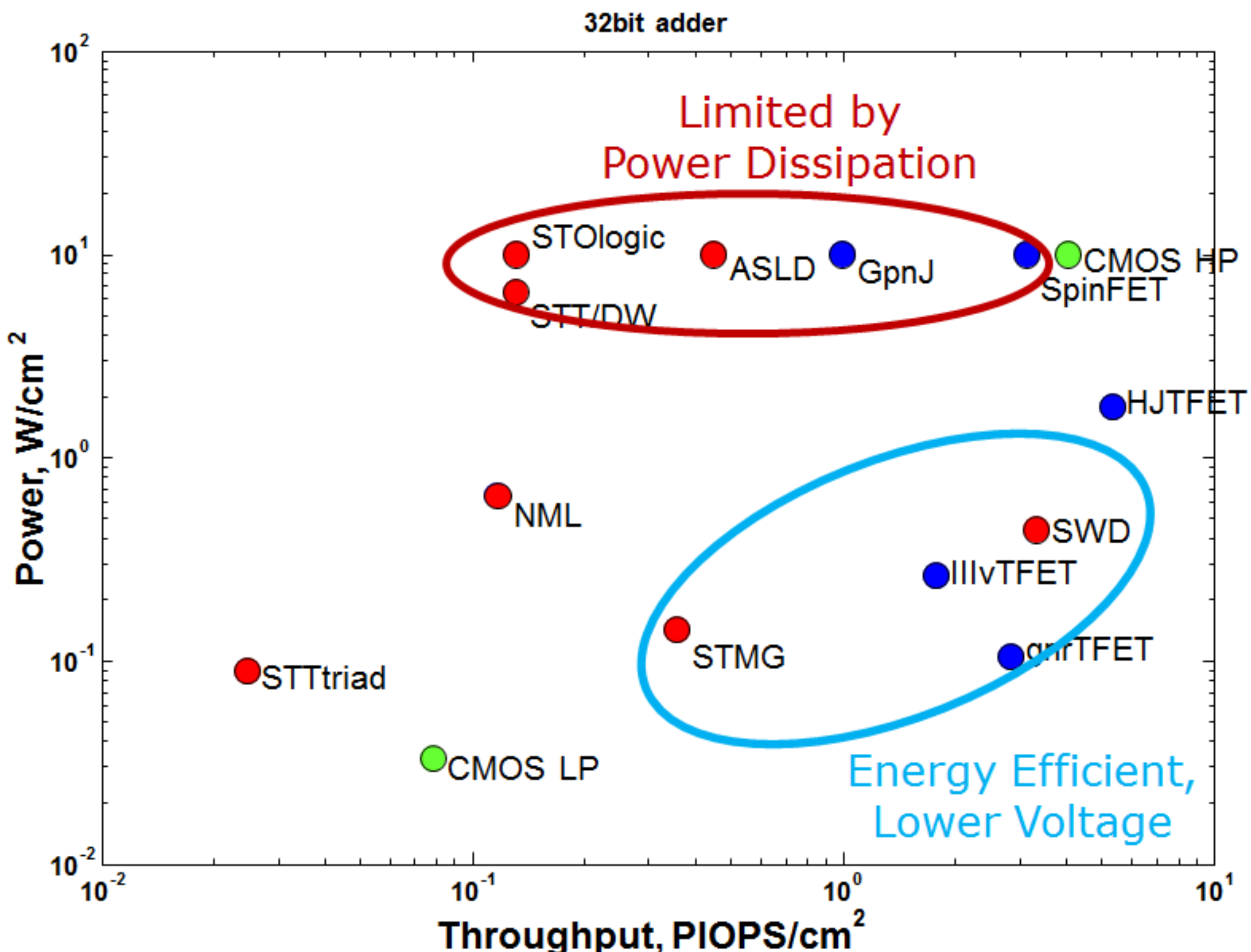
[Beyond CMOS]

Energy vs Delay – 32-bit adder



[Beyond CMOS]

Throughput vs Power – 32-bit adder



[Beyond CMOS]

Summary

device name	Area	Delay	Energy	Power	Throughput	Thr@<10W/cm^2
units	μm^2	ps	fJ	W/ cm^2	Pops/s/ cm^2	Pops/s/ cm^2
CMOS HP	40.8	84	2.48	71.8	29.00	4.04
CMOS LP	40.8	31331	0.42	0.0	0.08	0.08
IIIvTFET	54.4	1378	0.15	0.2	1.33	1.33
HJTFET	54.4	461	0.33	1.3	3.98	3.98
gnrTFET	54.4	861	0.04	0.1	2.13	2.13
GpnJ	26.2	143	10.03	268.0	26.73	1.00
SpinFET	40.8	282	3.20	27.8	8.68	3.13
STT/DW	6.8	112820	50	6.5	0.13	0.13
STMG	5.9	38094	0.40	0.2	0.44	0.44
STTtriad	17.7	228580	3.64	0.1	0.02	0.02
STOlogic	5.9	69760	51	12.3	0.24	0.20
ASLD	3.9	52522	20.78	10.0	0.48	0.48
SWD	2.0	12404	0.13	0.5	4.10	4.10
NML	11.8	57600	3.47	0.5	0.15	0.15

[Beyond CMOS]