

MASSACHUSETTS INSTITUTE OF TECHNOLOGY  
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

**6.111 Introductory Digital Systems Laboratory**  
Fall 2008

Lecture PSet #6  
*Due: Thu, 09/25/08*

**Problem 1.** Consider the following Verilog module that uses Euclid's algorithm to iteratively compute the greatest common divisor of two 16-bit unsigned integer values  $A_{in}$  and  $B_{in}$  where  $A_{in} \geq B_{in}$ .

```
module gcd(clk,start,Ain,Bin,answer,done);
  input clk,start;
  input [15:0] Ain,Bin;
  output reg [15:0] answer;
  output reg done;

  reg [15:0] a,b;
  always @ (posedge clk) begin
    if (start) begin a <= Ain; b <= Bin; done <= 0; end
    else if (b == 0) begin answer <= a; done <= 1; end
    else if (a > b) a <= a - b;
    else b <= b - a;
  end
endmodule
```

Please neatly complete the timing diagram below as the module computes the gcd of 21 and 15. Use “???” to indicate values that cannot be determined from the information given.

