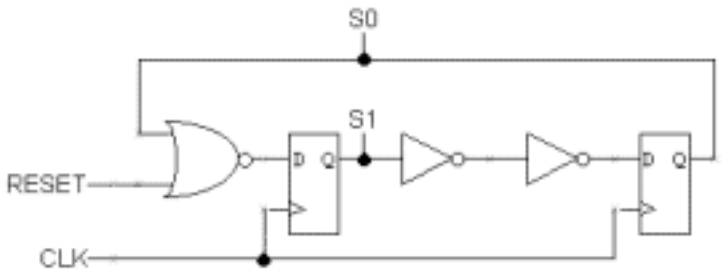
M A S S A C H U S E T T S I N S T I T U T E O F T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2008

Lecture PSet #4
Due: Thu, 09/18/08

Problem 1. Consider the following circuit diagram: S0 and S1:



inverter: t_{CD}=1ns, t_{PD}=2ns
nor2: t_{CD}=1.5ns, t_{PD}=2ns
D register: t_{CD}=0ns, t_{PD}=2ns, t_H=1ns, t_S=3ns

(A) What is the smallest clock period for which the circuit still operates correctly?

(B) A sharp-eyed student suggests optimizing the circuit by removing the pair of inverters and connecting the Q output of the left register directly to the D input of the right register. If the clock period could be adjusted appropriately, would the optimized circuit operate correctly? If yes, explain the adjustment to the clock period that would be needed.

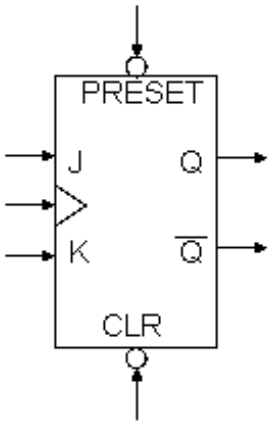
(C) When the RESET signal is set to "1" for several cycles, what values are loaded into the registers? (Give values for S0 and S1.)

(D) Assuming the RESET signal has been set to "0" and will stay that way, what value will with the registers have after the next clock edge assuming the current values are S0=1 and S1=1?

(E) Now suppose there is skew in the CLK signal such that the rising edge of CLK always arrives at the left register exactly 1ns before it arrives at the right register. What is the smallest clock period for which the FSM still operates correctly?

(see other side)

Problem 2. The figure and truth table below describe a positive-edge triggered J-K flip-flop with active-low *asynchronous* preset and clear.



Inputs					Outputs	
preset	clear	clk	J	K	Q	Qbar
0	X	X	X	X	1	0
1	0	X	X	X	0	1
1	1	no edge	X	X	Q	Qbar
1	1	↑	0	0	Q	Qbar
1	1	↑	1	0	1	0
1	1	↑	0	1	0	1
1	1	↑	1	1	toggle	

Write a Verilog module that implements the J-K flip-flop described above.