

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2008

Lecture PSet #3
Due: Tue, 09/16/08

Problem 1. A 3:1 multiplexer has the following inputs and output:

three data inputs D0, D1 and D2
two select inputs S0 and S1
one data output Y

The value of output Y is determined as follows:

Y = D0 if S0 = 0 and S1 = 0
Y = D1 if S0 = 1 and S1 = 0
Y = D2 if S1 = 1 (the value S0 doesn't matter)

- (A) Write a Verilog module for the 3:1 multiplexer that implements the sum-of-products equation for Y: $Y = \overline{S_0} \cdot \overline{S_1} \cdot D_0 + S_0 \cdot \overline{S_1} \cdot D_1 + S_1 \cdot D_2$. Use a dataflow style for your code (ie, use Boolean operators and use "assign" to set the values of your signals).
- (B) Write a Verilog module for the 3:1 multiplexer that uses the "?" conditional expression operator. Again use a dataflow style for your code (ie, use "assign" to set the values of your signals).
- (C) Write a Verilog module for the 3:1 multiplexer that uses the "case" statement. Make sure your implementation is strictly combinational, i.e., there's no unintentional creation of state. Note that the specification in this problem is slightly different than the mux3 example given in lecture, so you can't just copy the lecture code ☹.

Problem 2. Using the Verilog parameterized module mechanism it's possible to write modules whose operations depends on parameters specified when the module is instantiated.

- (A) Write a parameterized parity module takes as input a bus whose size is set by a parameter. The module has a single output which is 1 if the number of 1's in the input vector is odd and 0 otherwise. Hint: if you xor all the bits together you'll produce the desired result.
- (B) How would one instantiate an instance of your module to compute parity on the 16-bit data bus DATA[15:0]?