M A S S A C H U S E T T S   I N S T I T U T E   O F   T E C H N O L O G Y
DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

6.111 Introductory Digital Systems Laboratory
Fall 2004

Quiz #1: October 1, 2004

Name ANSWER KEY	*Score* *(out of 100)*

Problem 1. (10 points)

Incredible Inverters Inc. (III) manufactures a line of inverters they are hoping to sell as combinational devices that obey the static discipline. Incredibly, the voltage transfer curve for every device they make is exactly the same:
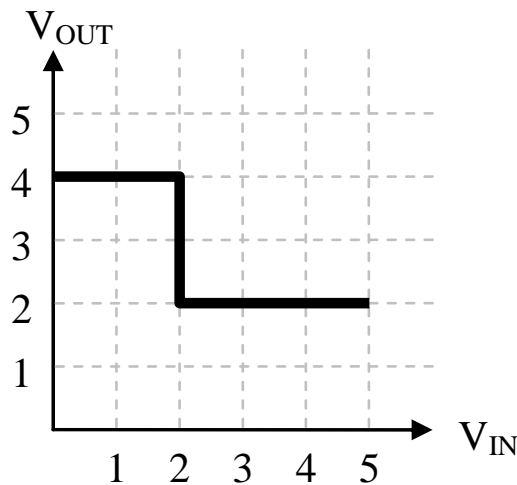
III would like for their devices to have the largest possible noise margins. Please specify choices for V_{OL}, V_{IL}, V_{IH} and V_{OH} that meet this goal, or briefly explain why devices with the given voltage transfer curve can't be used as combinational devices with positive noise margins.

Briefly explain why device can't be used or specify voltage levels: V_{OL} _____

V_{IL} _____

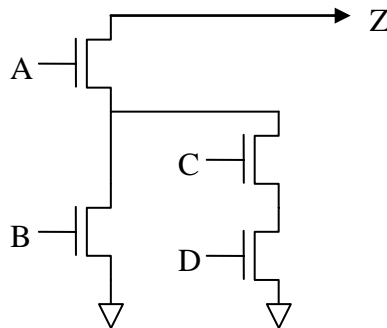V_{IH} _____

V_{OH} _____

This inverter can't have positive noise margins: from the diagram we see that Vol ≥ 2V, thus a positive noise margin requires Vil > 2V. But when Vin > 2V, Vout = 2V. So there would be valid input "0"s that wouldn't produce a valid "1" on the output.
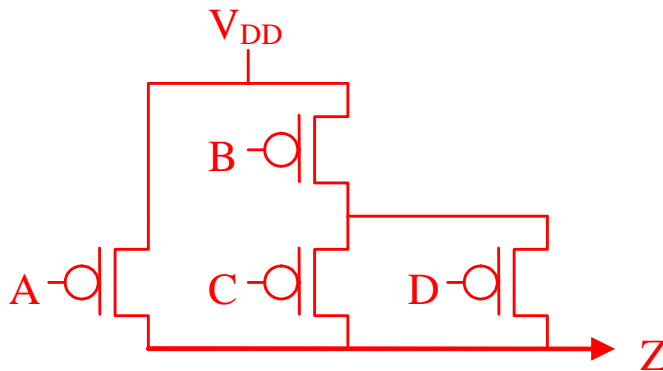
Problem 2. (20 points)

The following circuit diagram shows the pulldown circuitry for a particular CMOS gate.

(A) (10 points) Please draw the schematic for the pullup circuitry that correctly completes the implementation of the CMOS gate.
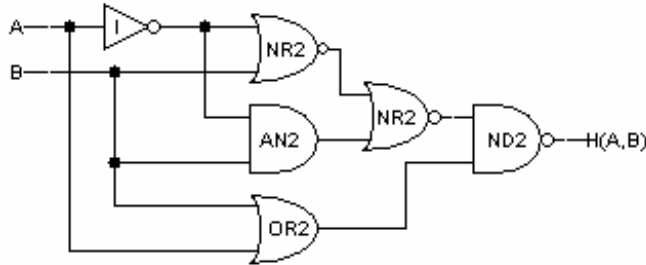
(Draw pullup schematic)

(B) (10 points) Assuming the pullup circuitry is designed correctly what is the function implemented by this gate?

Function implemented by gate: Z = $\overline{A \cdot (B + C \cdot D)}$

Problem 3. (20 points)

Consider the following circuit that implements the 2-input function H(A,B):

(A)   (12 points) Fill in the following truth table for H:

(Fill in truth table)

A	B	H
0	0	1
0	1	1
1	0	1
1	1	0

(B)   (4 points) Give a sum-of-products expression that corresponds to the truth table above. (Your expression does not have to be the minimal sum-of-products.)

Sum-of-products expression: H = $\overline{A \cdot B}$ _____

(C)   (4 points) Using the following table of timing specifications for each component, what are t_{CD} and t_{PD} for the circuit shown above?

gate	t_{CD}	t_{PD}
I	3ps	15ps
ND2	5ps	30ps
AN2	12ps	50ps
NR2	5ps	30ps
OR2	12ps	50ps

t_{CD} for circuit above (ps): 15ps _____

t_{PD} for circuit above (ps): 125ps _____

Tcd = smallest sum of Tcds along paths from inputs to the output
    = Tcd,nr2 + Tcd,nr2 + Tcd,nd2

Tpd = largest sum of Tpds along paths from inputs to the output
   = Tpd,inv + Tpd,an2 + Tpd,nr2 + Tpd,nd2

Problem 4. (20 points)

Consider the following truth table for F(A,B,C):

A	B	C	F(A,B,C)
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

(A) (6 points) Implement F(A,B,C) using only the 4-to-1 multiplexer shown below by labeling each of its six inputs with one of the constants 0 and 1; the inputs A, B, C, or their inversions $\overline{A}$, $\overline{B}$ and $\overline{C}$.

C → 00
C → 01
C → 10   → F(A,B,C)
1 → 11
A
B
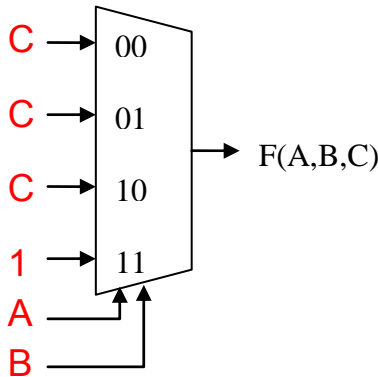
(B) (8 points) Fill in the template below to create a Karnaugh map for F(A,B,C). Be sure to label the rows and columns.

AB

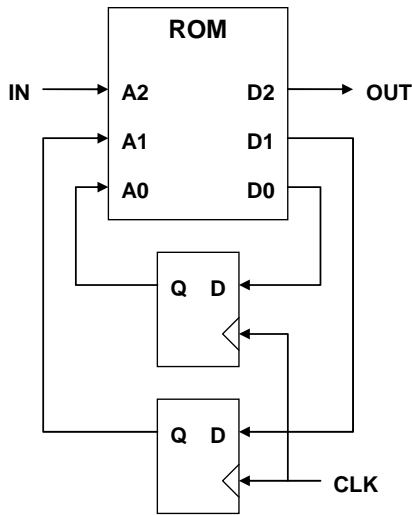|	00	01	11	10
C 0	0	0	1	0
1	1	1	1	1
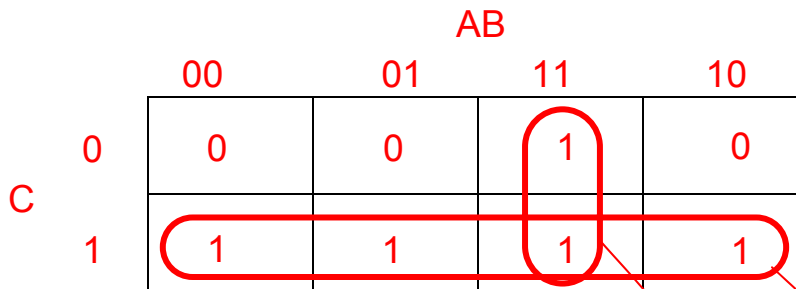
(C) (6 points) Give a minimal sum of products expression for F(A,B,C).

Minimal sum of products expression: F(A,B,C) = A•B + C

Problem 5. (30 points)

Consider the following diagram of a finite state machine. The table on the right gives the contents of the ROM. You may assume that transitions on IN are timed so as to meet the setup and hold times of the registers.
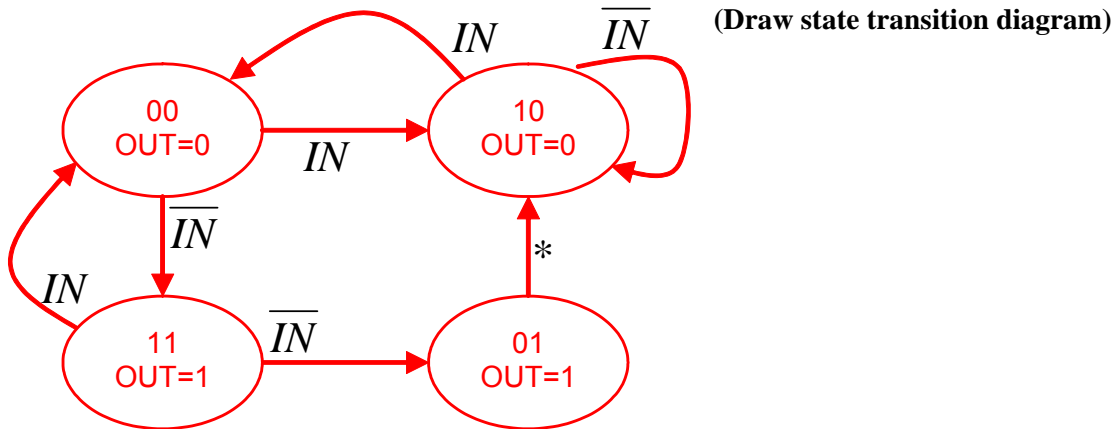
ROM Contents:

A2	A1	A0	D2	D1	D0
0	0	0	0	1	1
0	0	1	1	1	0
0	1	0	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	1	1	1	0
1	1	0	0	0	0
1	1	1	1	0	0

ROM diagram with inputs IN→A2, A1, A0 and outputs D2→OUT, D1, D0 feeding two registers (Q D) clocked by CLK.

Timing info:
  ROM: $T_{PD} = 4ns$, $T_{CD} = ?$
  REG: $T_{PD} = 1.5ns$, $T_{CD} = 0.5ns$
    $T_{SETUP} = 3ns$, $T_{HOLD} = 1.5ns$

(A) (14 points) Draw the state transition diagram for the finite state machine implemented by the circuit above. Be sure to label all the transition arcs and states with the appropriate values for IN and OUT.

(Draw state transition diagram)

State transition diagram:
- State 00 (OUT=0)
- State 10 (OUT=0)
- State 11 (OUT=1)
- State 01 (OUT=1)

Transitions: 00 →IN→ 10; 00 →$\overline{IN}$→ 11; 10 →IN→ 00; 10 →$\overline{IN}$→ 10 (self loop); 11 →IN→ 00; 11 →$\overline{IN}$→ 01; 01 →*→ 10.

(B) (8 points) Using the timing information given above, what are the constraints on the ROM's contamination delay that ensure the circuit operates correctly?

Tcd,reg + Tcd,rom ≥ Thold,reg

Constraints on $T_{CD,ROM}$: **≥ 1.0ns**

(C) (8 points) Using the timing information given above, what are the constraints on the period of CLK that ensure the circuit operates correctly?

Constraints on T_{CLK}: **≥ 8.5ns**

Tpd,reg + Tpd,rom + Tsetup,reg ≤ Tclk