Radio 6.111–An FPGA Implementation of a Software Radio

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November 4, 2005

This project intends to construct an implementation of an AM radio receiver using the Virtex II FPGA, an activated antenna and the SA612 balanced mixer/oscillator chip. It will employ a heterodyne architecture, using an oscillator signal to filter and tune the signal from the antenna, and pass it on to the digital signal processing core of the system. This radio will take in RF signals of frequencies ranging from 525 kHz to 1715 kHz. An ideal radio with a digital signal processing core would need to process signals at twice the highest frequency signal it would receive; this limits our practical ability to receive signals. As the Virtex II has an effective speed of 100 MHz, the signals that the labkit can process are theoretically limited to roughly 50 MHz. This allows listening to the AM band, but no higher. This project will also explore the feasibility of heterodyning the received signal, to allow receptions of higher-frequency radio signals.

It is possible to test the functionality of the system by listening to the output of the radio. There are six major modules involved in constructing this circuit amplifier, the mixer and oscillator, the analog-digital converter and the digital signal processor. There is also a minor module in the form of the antenna. As either hardware or Verilog implementations of many of these modules already exist, it will be possible to bootstrap this project upwards, building one module at a time while retaining functionality of the overall system.

The antenna will simply be a length of wire, wrapped into a coil of a specific number of turns and length to tune it to the proper frequency. If necessary, this piece of equipment can be purchased or constructed with wire-wrapping tools.

The amplifier can also be implemented using analog electronics; a few op-amps will be sufficient to construct this module in hardware. It is unknown whether digital signal amplification will be adequate in this application; more research needs to be done on this topic. The amplifier will take in the signal from the tuner and amplify it; this will allow greater clarity in the audio output of the system.

The tuner will be a simple band-pass filter, connected to the antenna; it will be keyed to the oscillator frequency, allowing the selection of a specific AM band. The author proposes that during the first stage of construction, the tuner is implemented using off-the-shelf analog components; as other modules are completed, this module will ideally be converted to a digital system. This will require moving the analog-to-digital

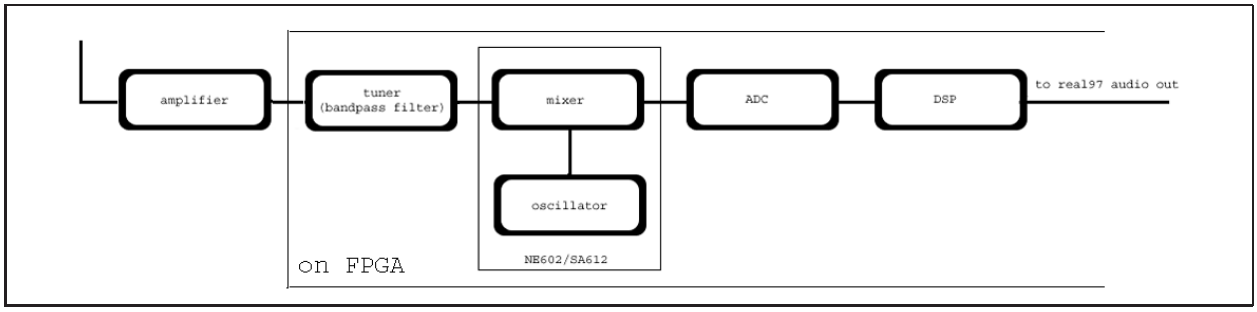

Figure 1: The diagram of the finite state machine.

converter farther forward in the chain, i.e. converting the signals received on all frequencies to digital samples and then filtering out the desired frequencies.

The mixer and oscillator complete the RF receiver front end; these modules already exist in the form of the NE602 and SA612 chips. Essentially, the functionality of these chips is to convert RF signals into IF signals that can be processed by the rest of the FPGA.

The analog-to-digital converter will sample the analog signals and convert those into digital information. It will be preceded by a small low-pass analog filter, to remove extraneous signals from higher frequencies. During the initial phase, the existing analog-to-digital infrastructure can be used; eventually, it is the goal of this project to design our own implementation of such a unit. Further filtering can be done at this phase, to enhance the signal, shape noise and deal with aliasing issues. Thus, the three separate portions of the signal processing unit can be an anti-aliasing filter, a noise-shaping filter and an additional amplifier. Demodulation can be handled by the Demodulation can be handled by the Real97 audio codecs; the digital samples will be fed into the labkit's built-in audio support.

This project aims to implement at least three of the six blocks in Verilog on the Virtex II FPGA–the tuner, the digital signal processor and the analog-to-digital converter, plus construction of a reliable antenna. These three systems are the bare minimum required for the radio to function as a digital system. As time and resources permit, the author would like to experiment with digital implementations of the oscillator and mixer; this may require implementing dedicated hardware to do real-time signal processing. The goal of this project is to complete the design and implementation of a software radio implemented on an FPGA within five weeks' time.