Radio 6.111–An FPGA Implementation of a Software Radio: Project Abstract

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This project intends to construct an implementation of an AM radio receiver with a digital signal processing core, using the Virtex II FPGA, an activated antenna and the SA612 balanced mixer/oscillator chip. An ideal radio with a digital signal processing core would need to process signals at twice the highest frequency signal it would receive; this limits our practical ability to receive signals. As the Virtex II has an effective speed of 100 MHz, the signals that the labkit can process are theoretically limited to roughly 50 MHz. This allows listening to the AM band, but no higher. This project will also explore the feasibility of heterodyning the received signal, to allow receptions of higher-frequency radio signals.

There are six major modules involved in constructing this circuit–the tuner, the amplifier, the mixer and oscillator, the analog-digital converter and the digital signal processor. There is also a minor module in the form of the antenna. As either hardware or Verilog implementations of many of these modules already exist, it will be possible to bootstrap this project upwards, building one module at a time while retaining functionality of the overall system. This project aims to implement at least three of the six blocks in Verilog on tthe Virtex II FPGA–the tuner, the digital signal processor and the analog-to-digital converter, plus construction of a reliable antenna. These three systems are the bare minimum required for the radio to function as a digital system. As time and resources permit, the author would like to experiment with digital implementations of the oscillator and mixer; this may require implementing dedicated hardware to do real-time signal processing.

The goal of this project is to complete the design and implementation of a software radio implemented on an FPGA within five weeks