Project Proposal
RFID Tag Reader System
MIT 6.111 – Introductory Digital Systems Laboratory
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Radio Frequency Identification (RFID) is an automatic identification technology that utilizes a tag, which may be passive (no internal power) or active (internal battery power), to allow encoded identification, location or other sensory data to be transmitted to a tag reader, which decodes and processes the information.

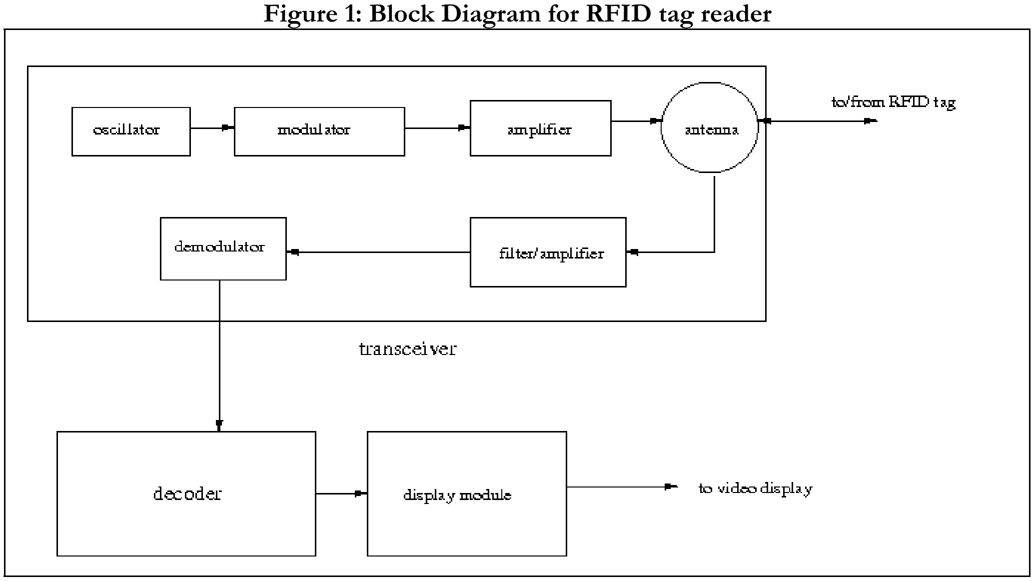
The RFID tag contains a transponder with a digital memory chip that possesses a unique ID, and an antenna to send and receive data to a reader. The RFID tag reader consists of an antenna, transceiver and decoder. The reader generates a continuous activation signal, and when a tag is within range of this signal, the tag sends the reader its identification.

Upon signal detection and identification of the tag, the tag reader then sends command signals to it. Responding to commands from the reader, the tag sends out encoded data. This data, which is sent out on a modulated frequency, is picked up and decoded by the reader, which sends it to a host computer to be processed.

System Description

The principal goal of this project is to successfully design, implement, and test a low-power, low-frequency (125 kHz) RFID tag reader for the passive RIFD tags in MIT ID cards. The tag reader system, which will be based on the 6.111 Xilinx FPGA labkit, will consist of three main subsystems: a transceiver, a decoder, and a display module. Figure 1 below shows a block diagram of the overall system.

Figure 1: Block Diagram for RFID tag reader



The transceiver's antenna will include a 125 kHz transmitter with low distortion for interrogation of tags, and a 62.5 kHz receiver to get the reply. Since the tag will send its data as an amplitude modulated (AM) signal, the reader will filter the signal to select and amplify the 62.5 kHz carrier, and demodulate it to get the signal transmitted by the tag. When it is done, it will flash a green LED to indicate successful reception.

The decoder will extract the data from the demodulated signal and perform the needed transformations on the data to get the identification data (MIT ID number).

Finally, the data will be sent to a video display module to generate the necessary signals to output the data to a display.

Design and Testing

This project will be implemented in three stages: design synthesis, design implementation, and product testing/verification. The first stage consists of conceptualizing ideas for an RFID tag reader design.

The second stage consists of taking the concepts developed and organizing them into a workable plan capable of implementation. This stage involves creating detailed functional specifications and required performance specifications. Clear specifications allow the construction of a block diagram for the tag reader, which displays each subsystem of the tag reader and the input/output dataflow paths between them. With a complete description of the functionality of each subsystem and their interactions, creation of the actual tag reader is possible.

As the tag reader is being built, it will undergo testing to confirm the functionality of each subsystem. This will be considered the third stage of implementation. When construction is complete, the entire system will undergo testing to confirm successful implementation.

Initially, operation of the reader's transceiver will be tested using an oscilloscope to verify the interrogation frequency. The individual modules of the tag reader, which will be programmed, compiled and run on the FPGA, will be tested for functionality by utilizing testbench simulations in a Verilog programming client. Once successful operation of the reader is verified in terms of generating and transmitting the appropriate data, its proper communication with the tag can then be verified via generating and confirming output from the tag, which will possess known values.

Division of Labor

The RFID tag reader project will be divided into two sections: data collection and data display. Data collection will consist employing the transceiver to send a signal to the tag and receive a reply from it. Both Katonio and Akua will work on the transceiver, since its successful construction is paramount to demonstrating initial system operability. Akua will work on the receiver part (filtering and demodulation), while Katonio will work on the transmitter (building the antenna, generating a 125 kHz signal).

The data display module consists of decoding the information from the signal and displaying it on a video screen. Katonio will write the code to display the numbers from the data on a video screen in a useful way. Akua will work on actually generating the numbers from the stream of data bits. Additionally, each individual module built in this phase will be tested many times over in an attempt to make the debugging process less daunting.

It is believed that through this division of labor scheme, an operational tag reader system can be successfully demonstrated by the end of the project period.