

BETA2

An implementation of the 6.004 Beta processor with a 2-stage pipeline (IF, EXE) and one annulled branch delay slot. Memory operations (LD/LDR/ST) require two cycles in the EXE stage: the address is computed in the first cycle, the memory access made in the second (during which $m_{sel}=1$ and the IF stage is stalled). Other instructions take a single EXE cycle. Other changes:

- branch and LDR address arithmetic is performed by the ALU adder. To simplify the PCSEL logic JMP addresses are also routed through the ALU.
- a single main memory port is multiplexed between instruction fetch ($m_{sel}=0$) and memory accesses ($m_{sel}=1$).
- since regfile read and write are in the same stage, no bypassing is needed.

