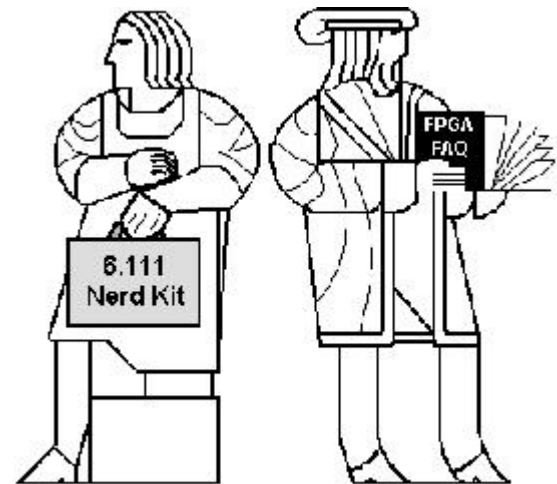


6.111 Lecture 14

Today: Analog Blocks

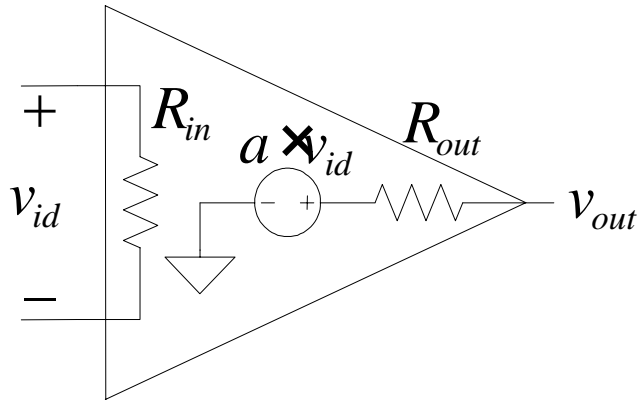
1. Op Amps
2. Conversion noise
3. Digital to Analog
4. Analog to Digital
5. Interfacing to FPGA's



Acknowledgements: Dave Wentzloff

1. Operational Amplifiers: an Introduction

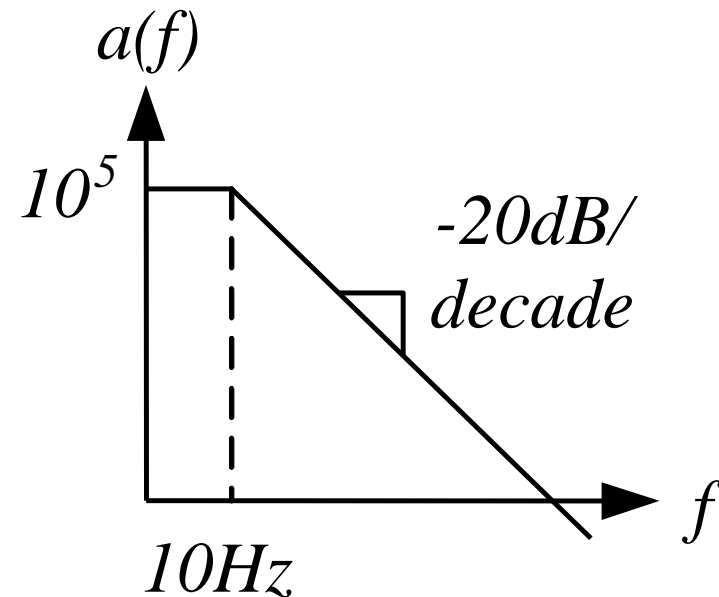
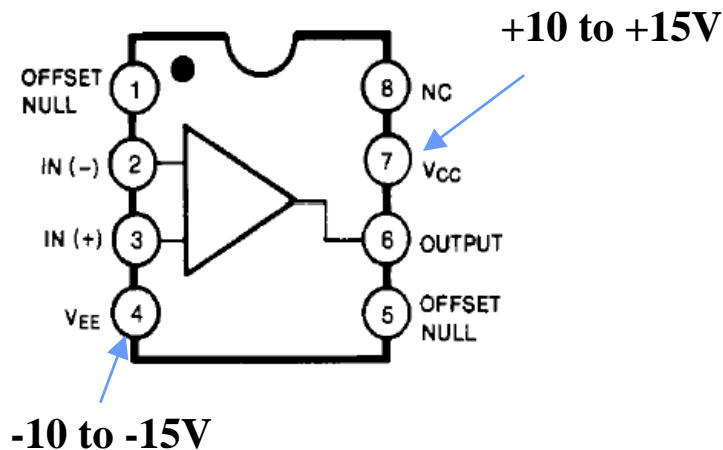
DC Model



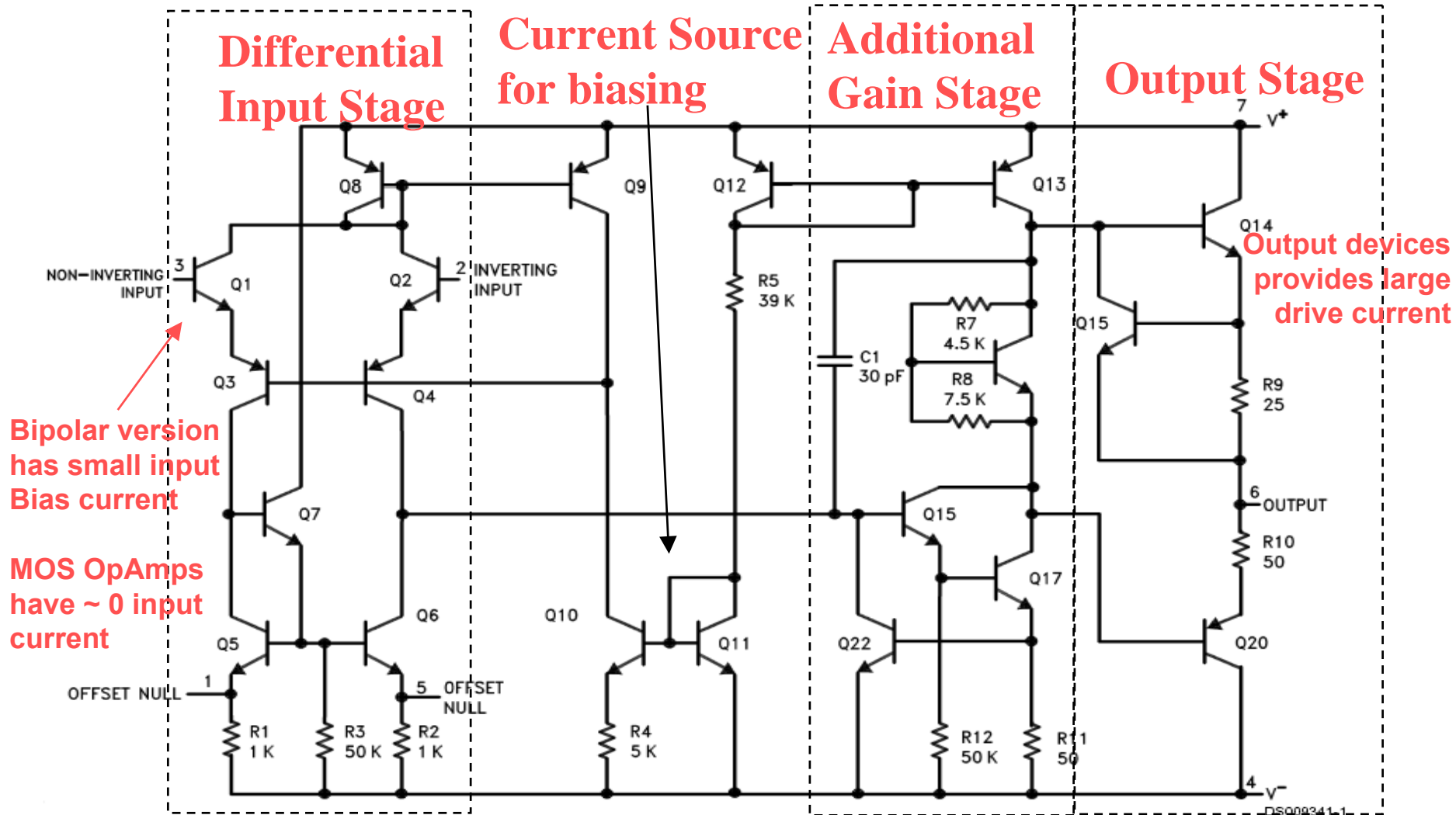
- Typically very high input resistance $\sim 300\text{K}\Omega$
- High DC gain ($\sim 10^5$)
- Output resistance $\sim 75\Omega$

$$V_{out} = a(f) \cdot V_{in}$$

LM741 Pinout

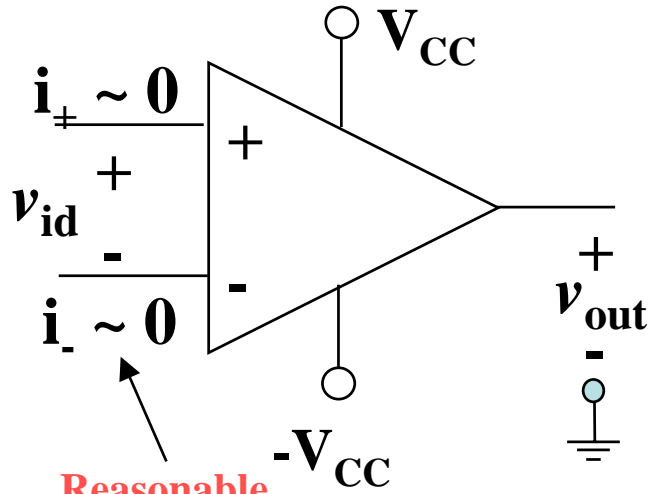


The Inside of a 741 OpAmp

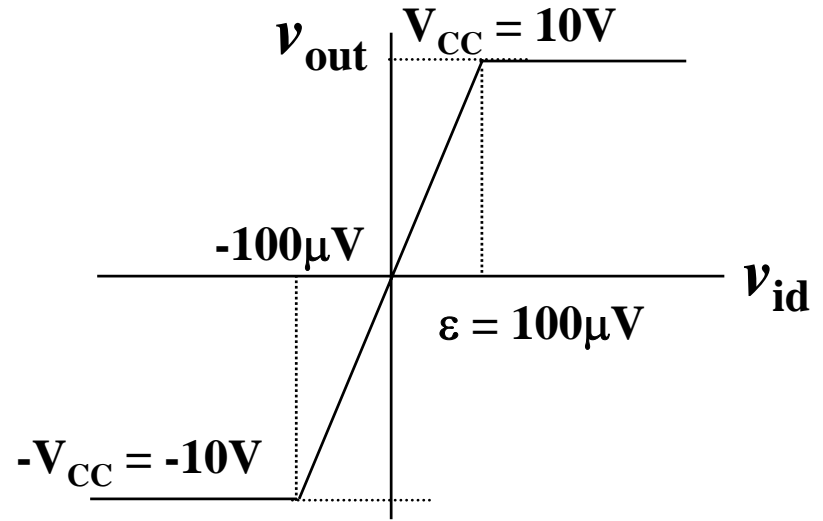


Gain is Sensitive to Operating Condition
(e.g., Device, Temperature, Power supply voltage, etc.)

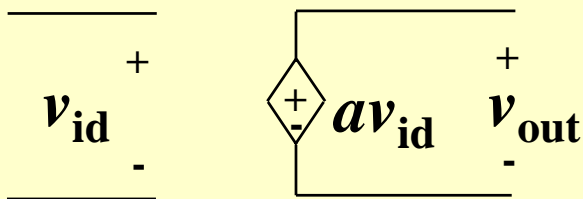
Simple Model for an OpAmp



Reasonable approximation

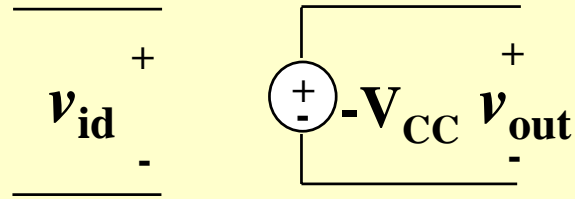


Linear Mode



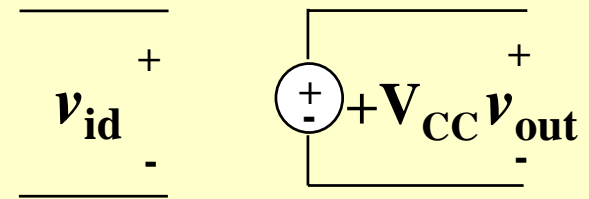
$$\text{If } -V_{CC} < v_{out} < V_{CC}$$

Negative Saturation



$$v_{id} < -\epsilon$$

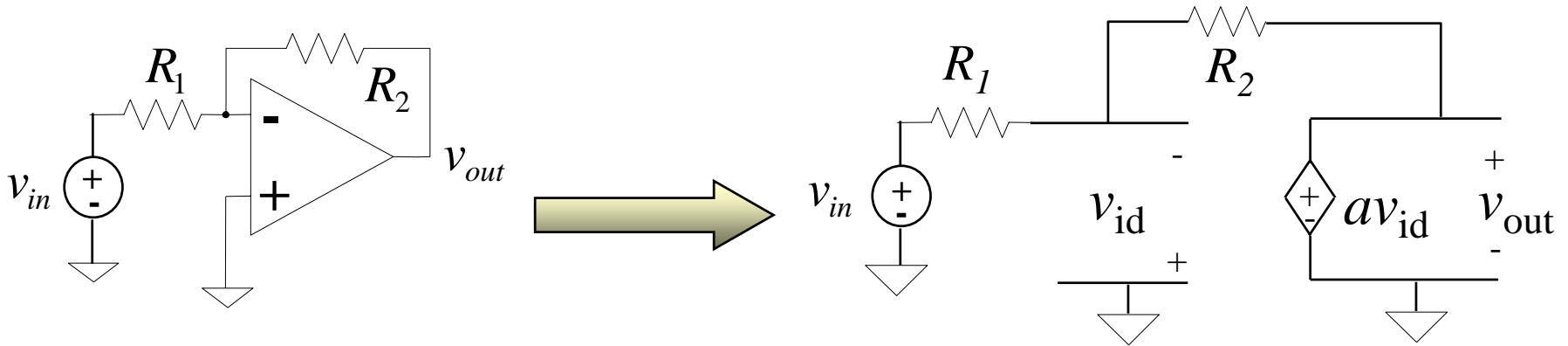
Positive Saturation



$$v_{id} > \epsilon$$

Very small input range for "open loop" configuration

The Power of (Negative) Feedback



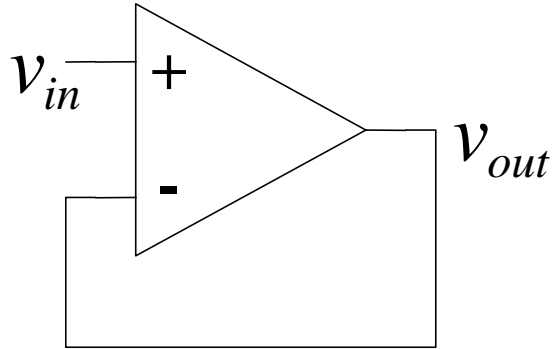
$$\frac{v_{in} + v_{id}}{R_1} + \frac{v_{out} + v_{id}}{R_2} = 0 \quad v_{id} = \frac{v_{out}}{a} \quad \frac{v_{in}}{R_1} = -\frac{v_{out}}{a} \left[\frac{1}{R_1} + \frac{a}{R_2} + \frac{1}{R_2} \right]$$

$$\frac{v_{out}}{v_{in}} = -\frac{R_2 a}{(1+a)R_1 + R_2} \approx -\frac{R_2}{R_1} \text{ (if } a \gg 1)$$

- Overall (closed loop) gain does not depend of open loop gain
- **Trade gain for robustness**
- Easier analysis approach: **"virtual short circuit approach"**
 - $v_+ = v_- = 0$ if OpAmp is linear

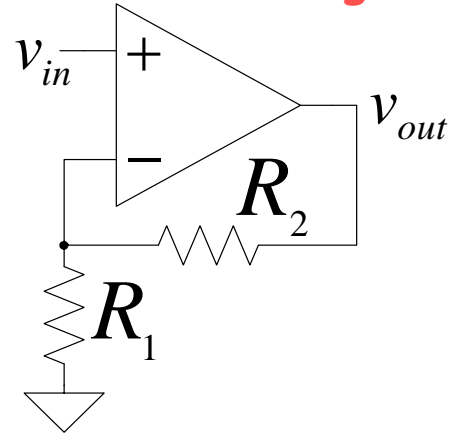
Basic OpAmp Circuits

Voltage Follower (buffer)



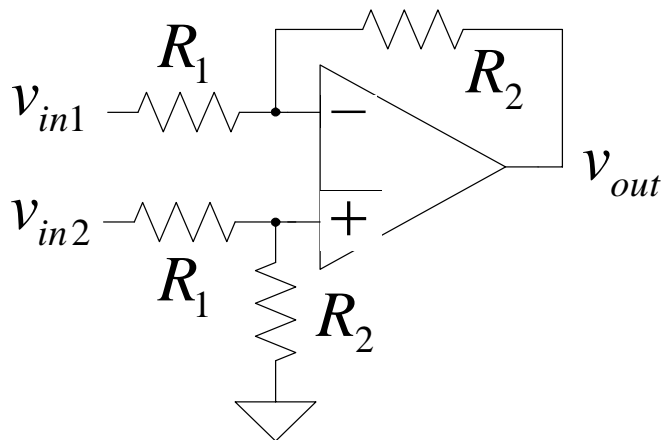
$$v_{out} \approx v_{in}$$

Non-inverting



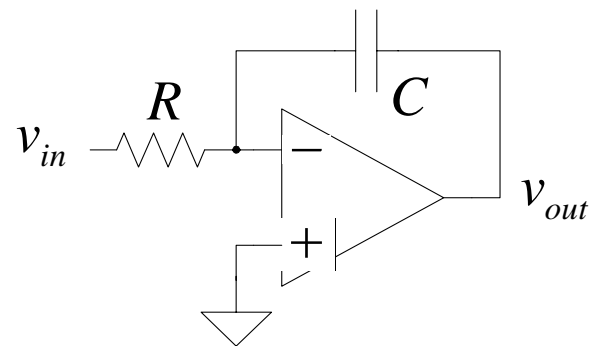
$$v_{out} \approx \frac{R_1 + R_2}{R_1} v_{in}$$

Differential Input



$$v_{out} \approx \frac{R_2}{R_1} (v_{in2} - v_{in1})$$

Integrator



$$v_{out} \approx -\frac{1}{RC} \int_{-\infty}^t v_{in} dt$$

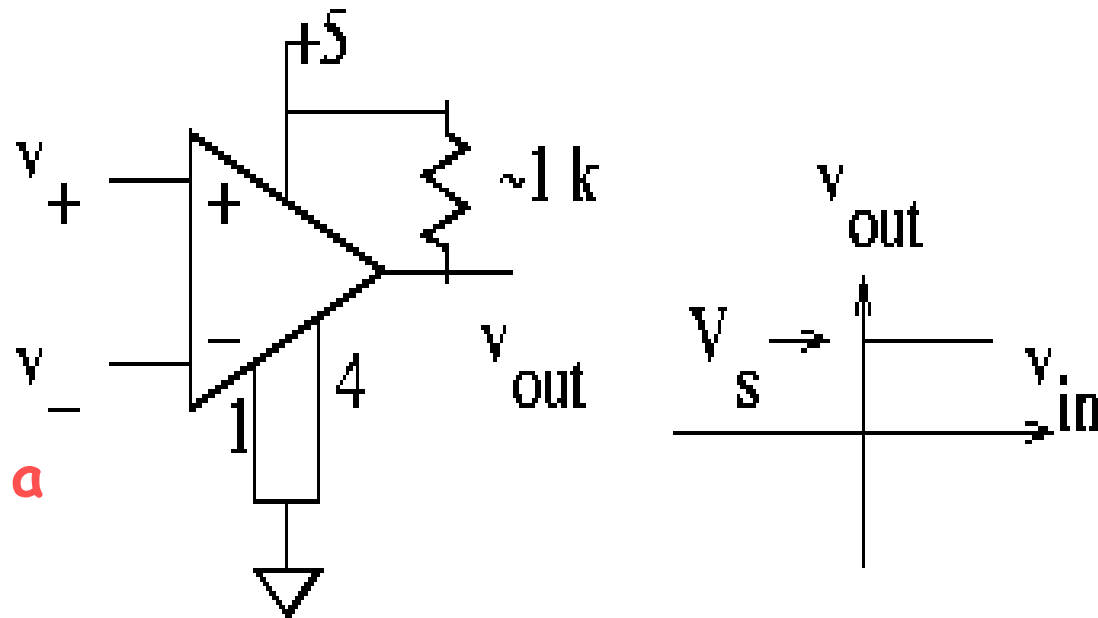
OpAmp as a Comparator

Analog Comparator:

Is $V_+ > V_-$? The Output is a DIGITAL signal

Analog Comparator: Analog to TTL

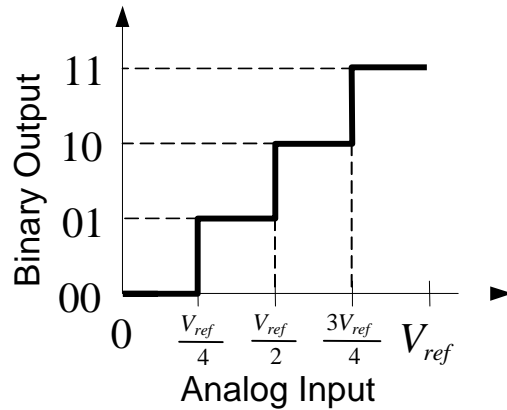
LM 311 Needs Pull-Up



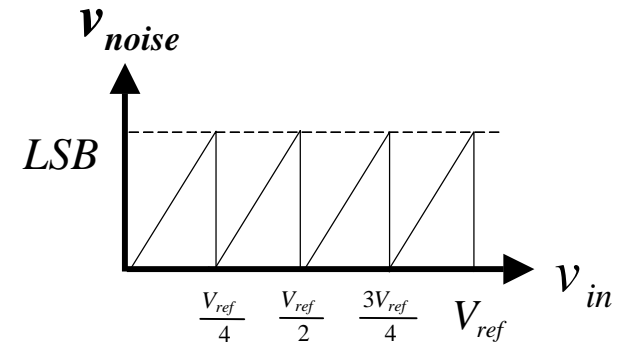
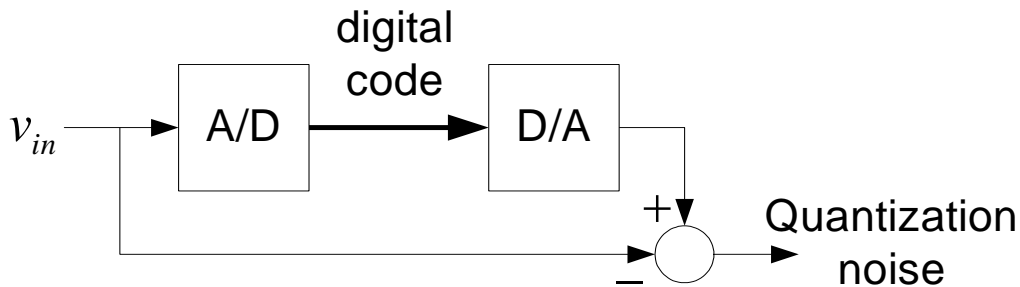
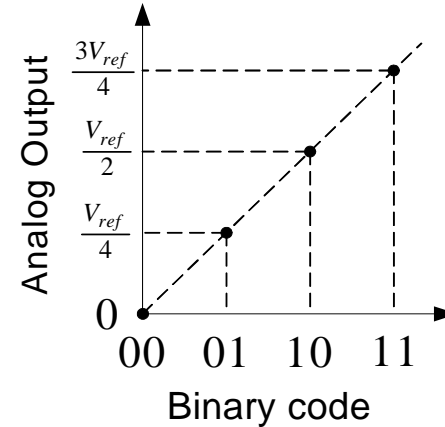
LM311 uses a single supply voltage

2. Data Conversion: Noise

A/D Conversion



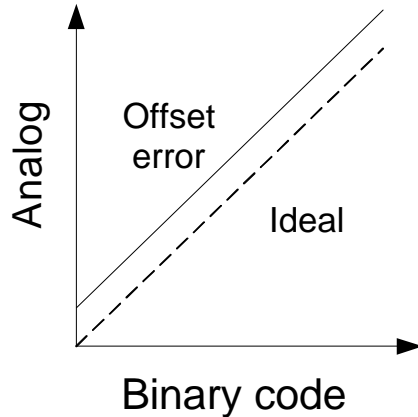
D/A Conversion



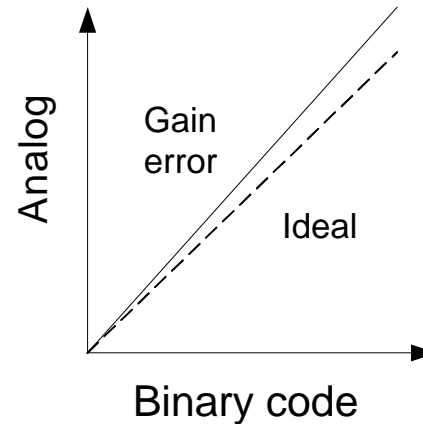
- Quantization noise exists even with *ideal* A/D and D/A converters

Non-idealities in Data Conversion

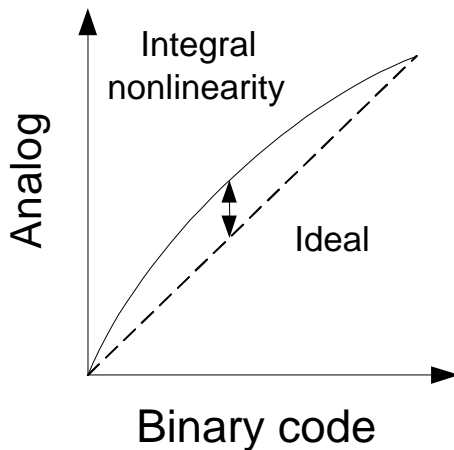
Offset - a constant voltage offset that appears at the output when the digital input is 0



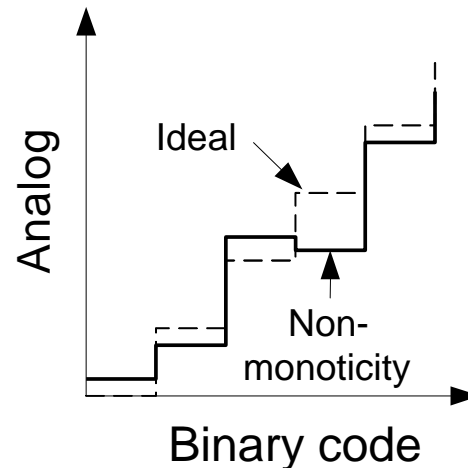
Gain error - deviation of slope from ideal value of 1



Integral Nonlinearity - maximum deviation from the ideal analog output voltage



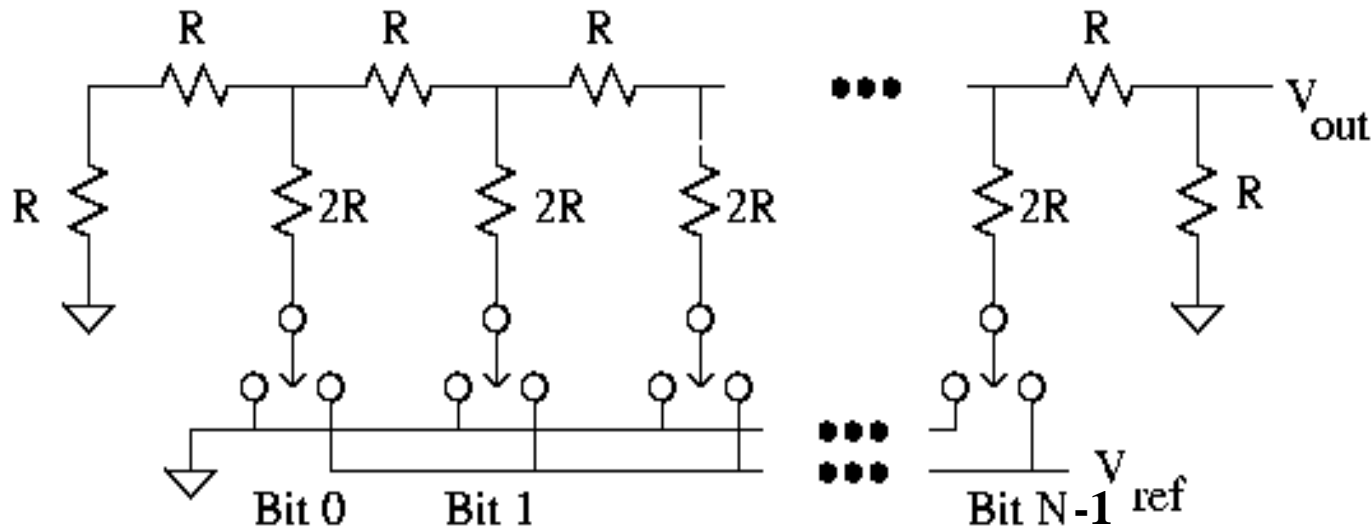
Differential nonlinearity - the largest increment in analog output for a 1-bit change



3. Digital to Analog

- **Common metrics:**
 - Conversion rate - DC to ~500 MHz (video)
 - # bits - up to ~24
 - Voltage reference source (internal / external; stability)
 - Output drive (unipolar / bipolar / current) & settling time
 - Interface - parallel / serial
 - Power dissipation
- **Common applications:**
 - Real world control (motors, lights)
 - Video signal generation
 - Audio / RF "direct digital synthesis"
 - Telecommunications (light modulation)
 - Scientific & Medical (ultrasound, ...)

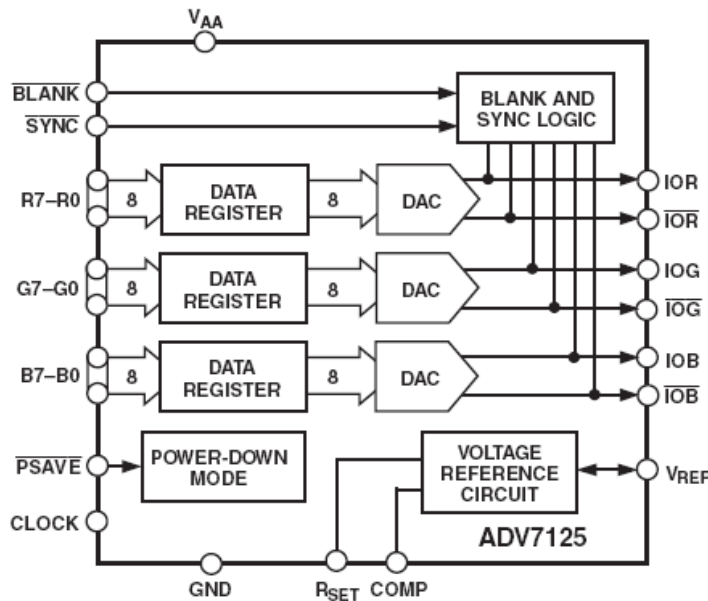
R-2R Ladder DAC Architecture



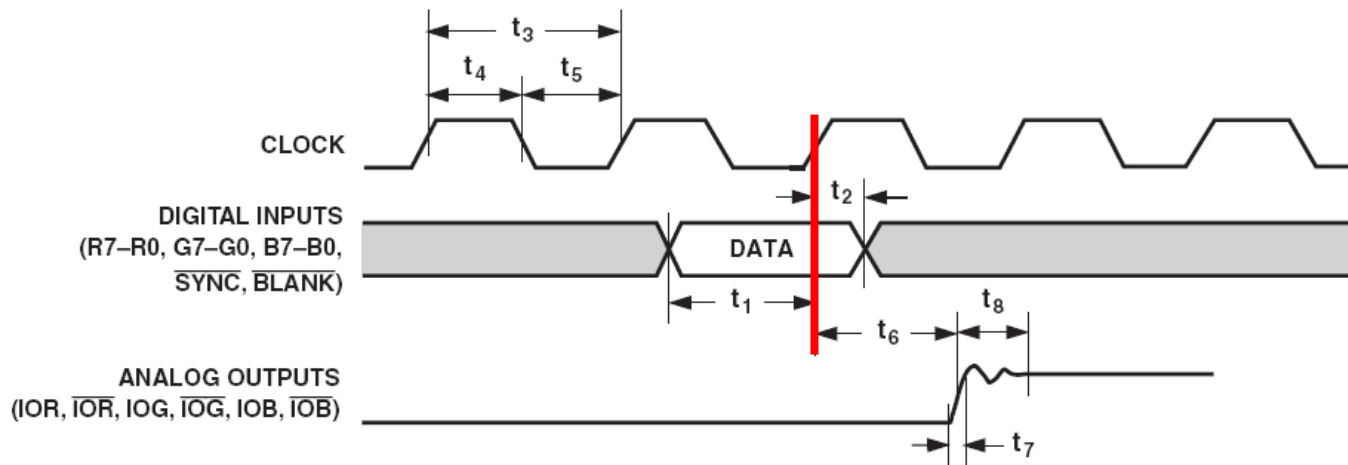
$$V_{out} = \frac{1}{6} V_{ref} \left[B_7 + \frac{1}{2} B_6 + \frac{1}{4} B_5 + \dots + \frac{1}{128} B_0 \right]$$

- Note that the driving point impedance (resistance) is the same for each cell.
- R-2R Ladder achieves large current division ratios with only two resistor values

Labkit: ADV7125 Triple Out Video DAC



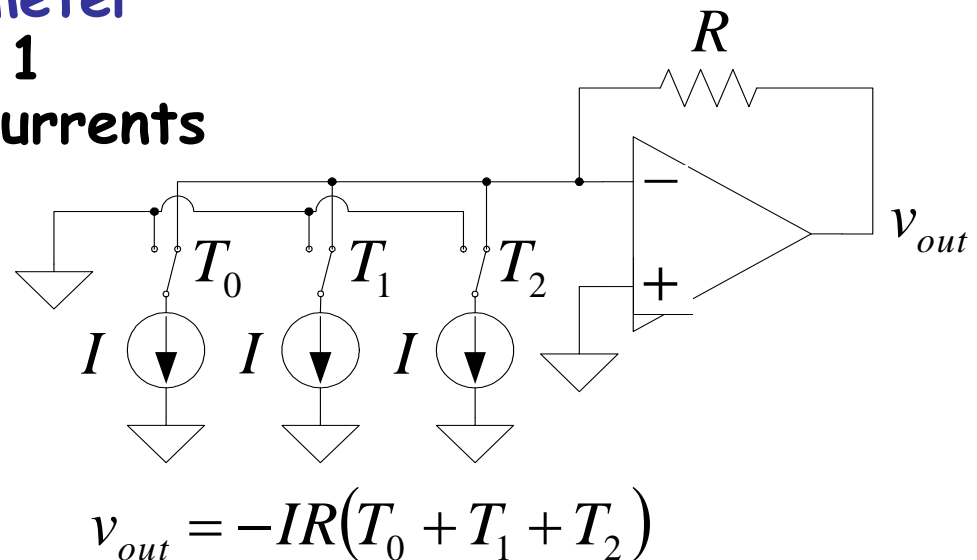
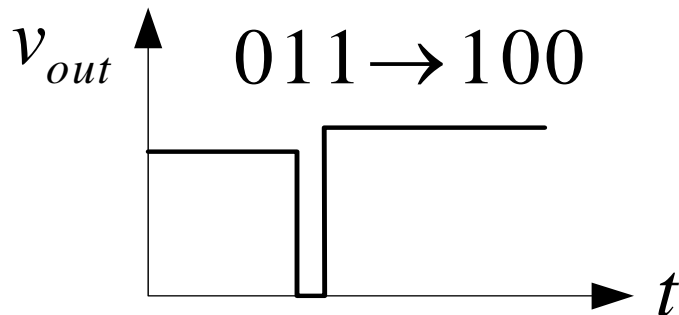
- Three 8-bit DACs
- Single Supply Op.: 3.3 to 5V
- Internal bandgap voltage ref
- Output: 2-26 mA
- 330 MSPS (million samples per second)
- Simple edge-triggered latch based interface



Glitching and Thermometer D/A

- **Glitching** is caused when switching times in a D/A are not synchronized
- **Example:** Output changes from 011 to 100 - MSB switch is delayed
- **Filtering** reduces glitch but increases the D/A settling time
- One solution is a **thermometer code D/A** - requires $2^N - 1$ switches but no ratioed currents

Binary		Thermometer		
0	0	0	0	0
0	1	0	0	1
1	0	0	1	1
1	1	1	1	1

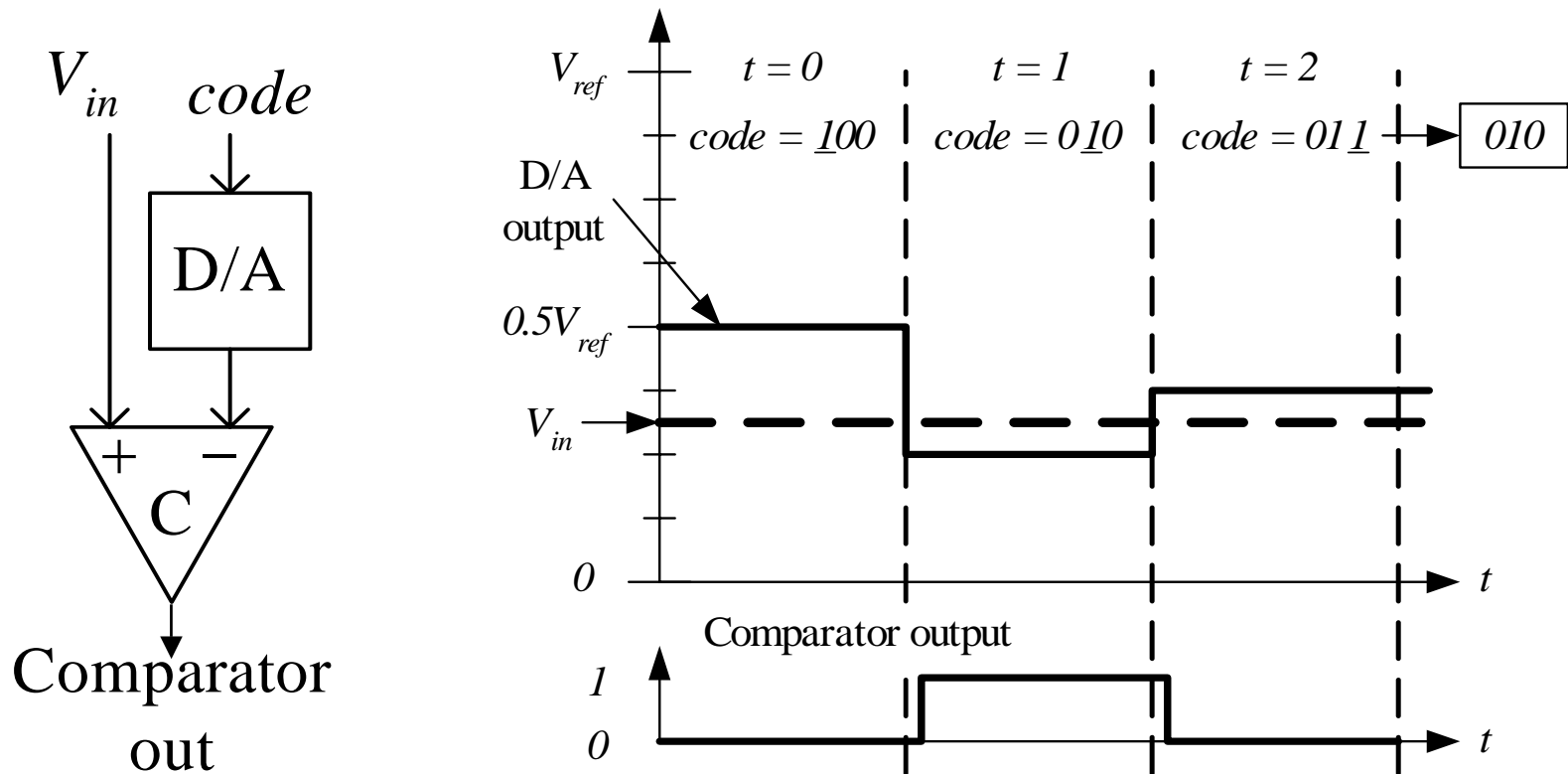


4. Analog to Digital

- **Common metrics:**
 - Conversion rate - DC to ~100 MHz
 - # bits - up to ~20
 - Input range - unipolar / bipolar
 - Interface - parallel / serial
 - Type: successive approximation, sigma-delta, flash
- **Common applications:**
 - Real world sensing (position, speed, force, temperature, ...)
 - Video signal digitization
 - Audio / RF recording & receiving
 - Telecommunications (light demodulation)
 - Scientific & Medical

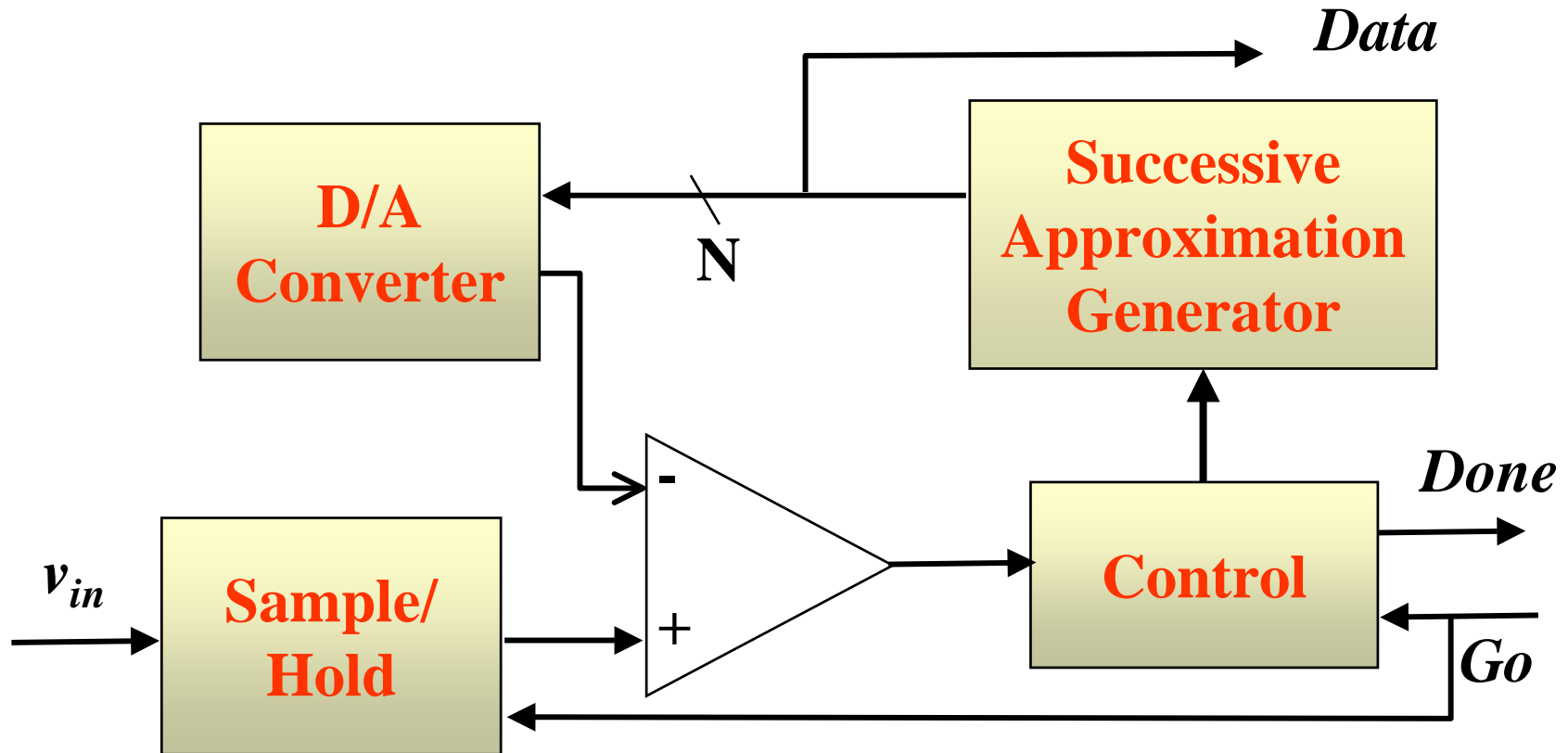
Successive-Approximation A/D

- D/A converters are typically compact and easier to design. Why not A/D convert using a D/A converter and a comparator?
- DAC generates analog voltage which is compared to the input voltage
- If DAC voltage > input voltage then set that bit; otherwise, reset that bit
- This type of ADC takes a fixed amount of time proportional to the bit length



Example: 3-bit A/D conversion, $2 \text{ LSB} < V_{in} < 3 \text{ LSB}$

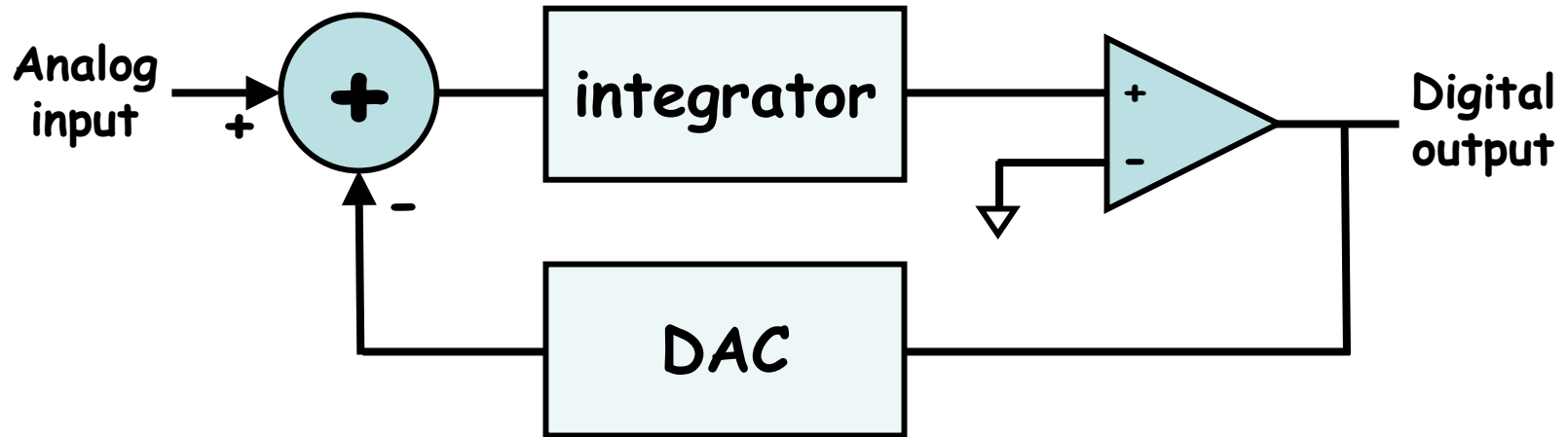
Successive-Approximation A/D



Serial conversion takes a time equal to $N(t_{D/A} + t_{comp})$

Sigma Delta ADC

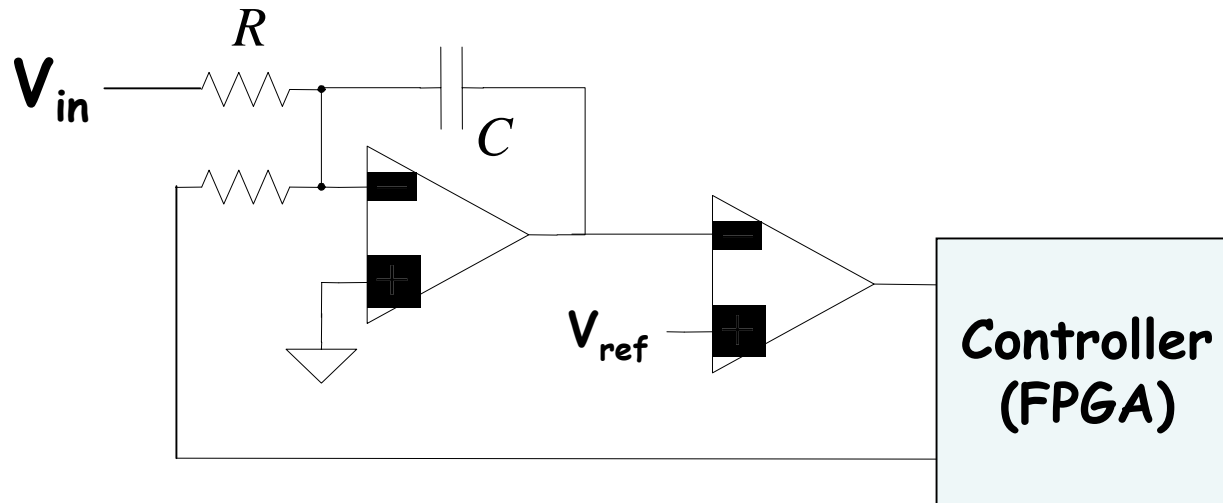
- Digitize differential signal:



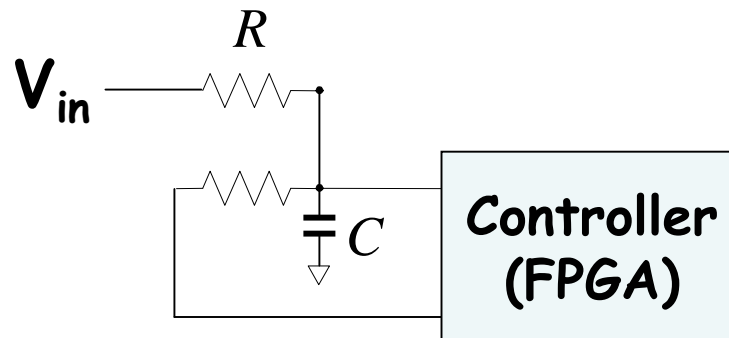
- "oversampled" at many times Nyquist frequency
- Frequency of 1's in digital output gives voltage

Sigma Delta ADC

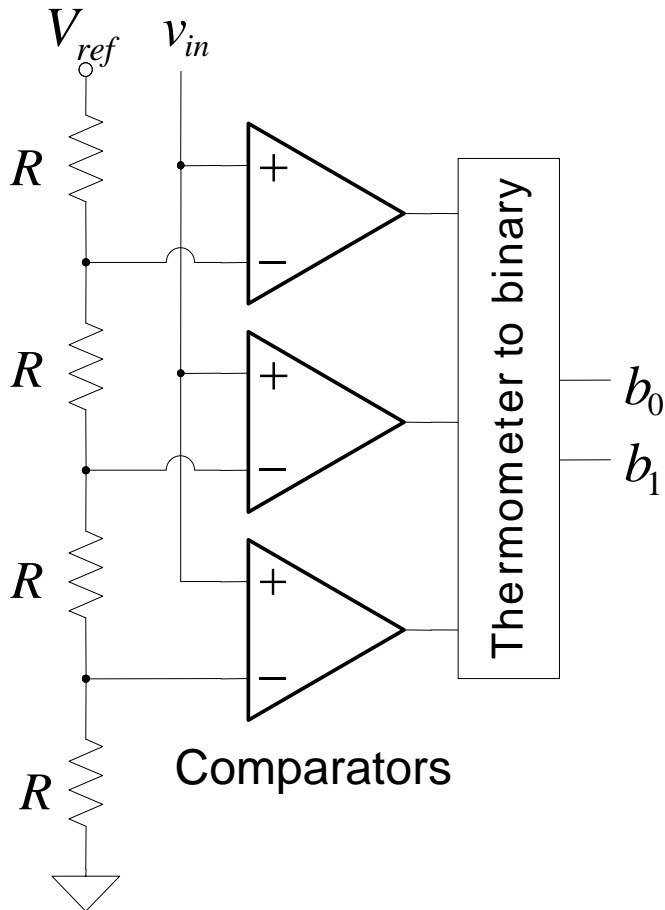
- A simple ADC:



- Poor Man's ADC:



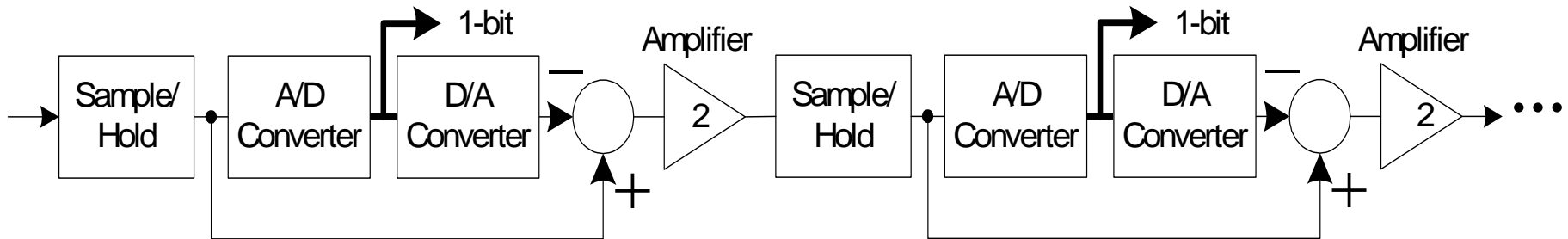
Flash A/D Converter



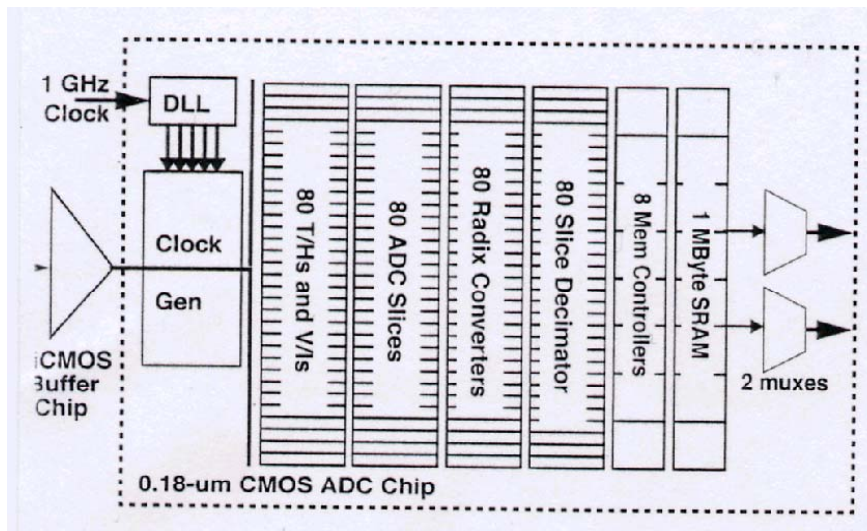
- Brute-force A/D conversion
- Simultaneously compare the analog value with every possible reference value
- Fastest method of A/D conversion
- **Size scales exponentially with precision**
(requires 2^N comparators)

High Performance Converters: Use Pipelining and Parallelism!

Pipelining (used in video rate, RF basestations, etc.)



Parallelism (use many slower A/D's in parallel to build very high speed A/D converters)



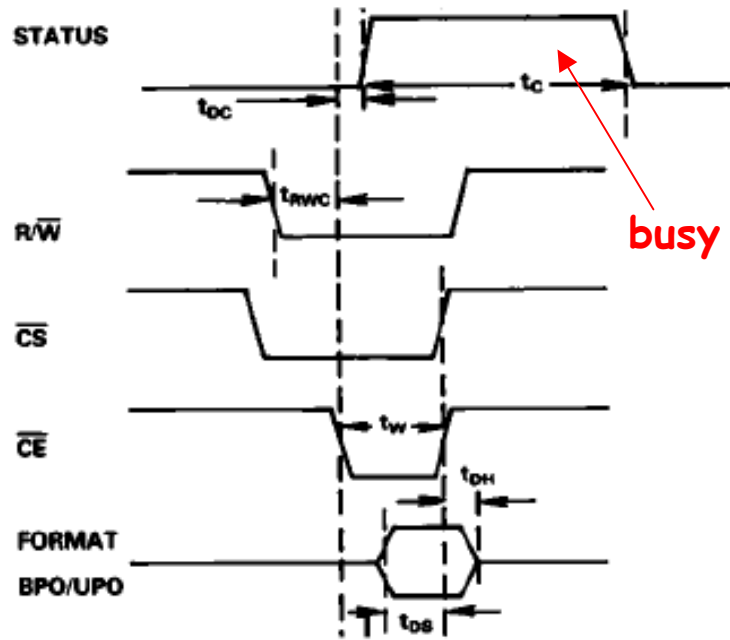
[ISSCC 2003],
Poulton et. al.

20Gsample/sec,
8-bit ADC
from Agilent Labs

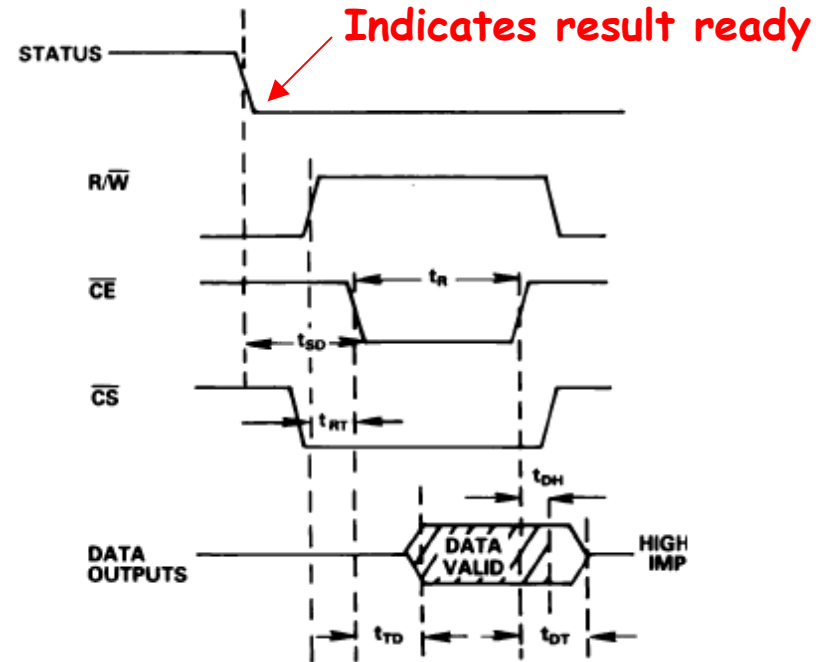
5. Interfacing to FPGA's

- Parallel (memory mapped peripheral)

Typical example: AD670 ADC

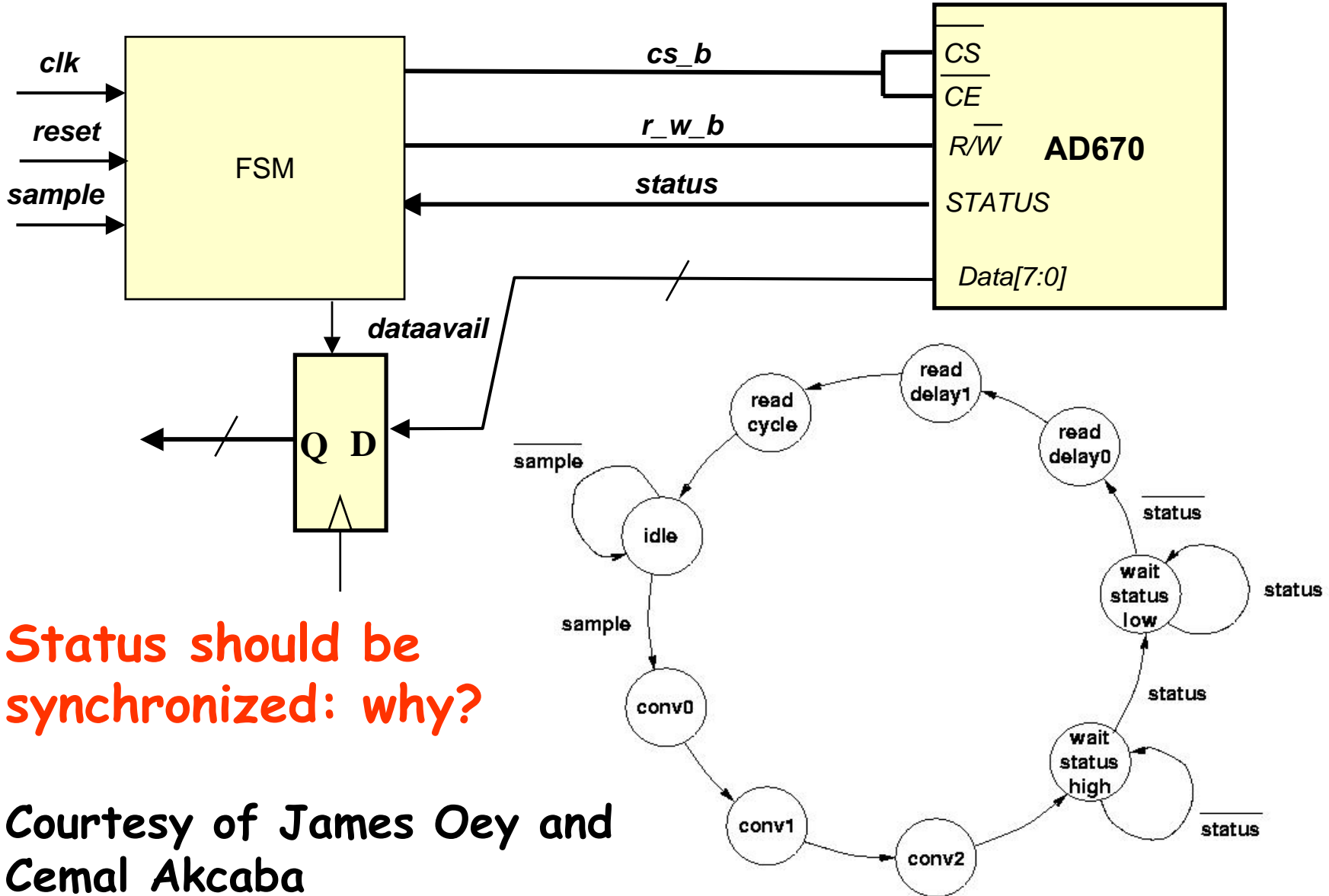


Start Conversion



Read Result

Simple A/D Interface FSM

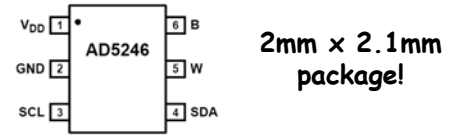


Status should be synchronized: why?

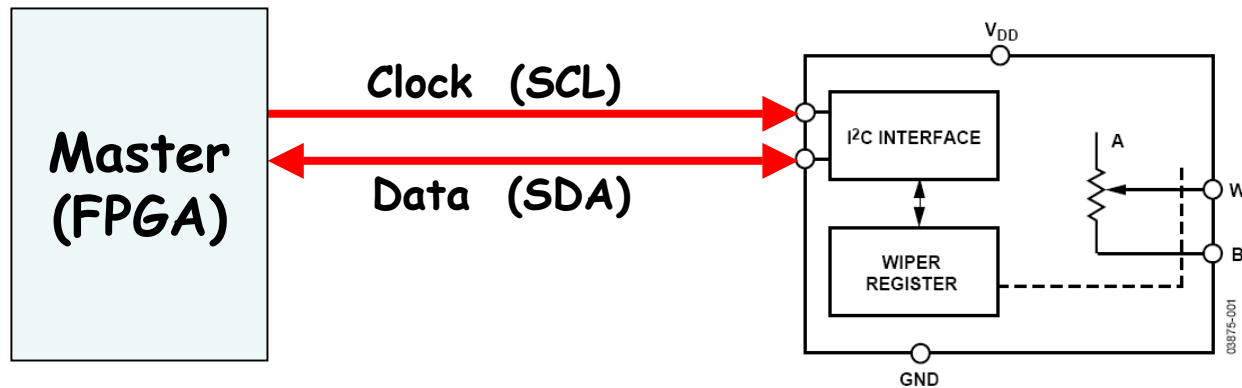
Courtesy of James Oey and Cemal Akcaba

Example: Digital Potentiometer

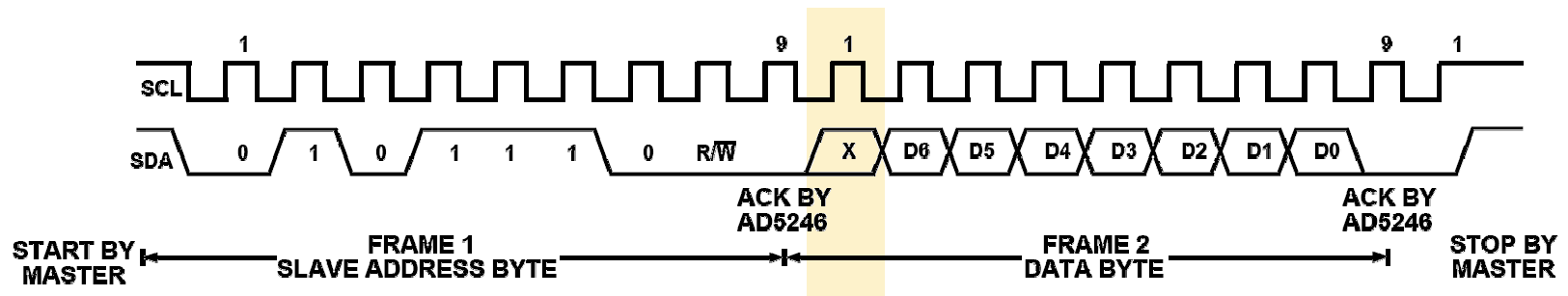
- AD5246 "128-position digital resistor



- I²C Serial bus: one master, multiple slave devices

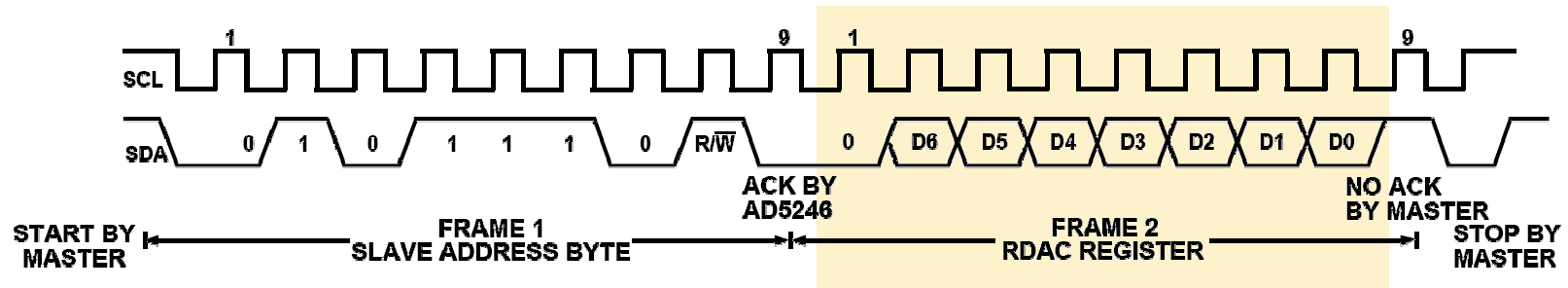


- Writing potentiometer setting:



Example: Digital Potentiometer

- Read potentiometer setting:



- Verilog

I2C interface

```
module i2c(clk,rdata,rd,wdata,wr,scl,sda);  
    input clk,rd,wr;  
    input [7:0] wdata;    output [7:0] rdata;  
    output scl;    inout sda;    reg dir,sdout;  
  
    assign sda = dir ? 1'bZ : sdout;  
    . . .  
endmodule
```

- Serial protocols: I²C, SPI, "one-wire"

Summary

- **OpAmps:**

- Basic elements of most conversion circuits
- Gain determined by ratios of resistances

- **DAC's:**

- R2R ladder ; fast operation

- **ADC's:**

- Successive Approximation, sigma-delta, flash
- Be sure to synchronize signals

- **Analog jellybean parts:**

- Digital potentiometers, I2C thermometers,...
- Use INOUT for bidirectional lines in verilog

